An 8 GHz digital spectrometer for millimeter-wave astronomy

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ABSTRACT

We have designed and tested a digital spectrometer suitable for analyzing 8 GHz baseband signals. It is based on a 16-Gsps, 5-bit ADC from e2v and a Stratix-IV FPGA employed for later filtering and signal processing. Digitized data is received and synchronized via twenty high-speed 4-Gbps transceivers integrated in the FPGA. A 64-channel polyphase filter bank separates the input signal into 250-MHz sub-bands, allowing subsequent high-resolution analysis. To obtain continuous spectral information over the input bandwidth, we have implemented a 50% overlapping architecture solution. Subsequently these sub-bands are processed using Fast Fourier Transform modules.

This system meets present-day demands on high-resolution wideband digital back-ends for millimeter-wave telescopes. This technology will be part of the next generation wideband correlator for the future upgrade of the IRAM Plateau de Bure interferometer (NOEMA project).

Keywords: digital spectrometer, high-resolution wideband back-ends, high-speed ADC, FPGA, polyphase filter banks

1. INTRODUCTION

Current digital back-ends for millimeter-wave astronomy are able to analyze wideband signals, while offering a flexible range of spectral resolutions. These back-ends are based on high-speed analog-to-digital converters (ADCs) and high-density field-programmable gate arrays (FPGA) devices. The present sampling rate of the ADCs and the computing power of the FPGAs make it possible to directly digitize analog signals of a few GHz of instantaneous bandwidth, and later to analyze them at high spectral resolutions up to a few tens of kHz.

In this paper, we describe the implementation of a digital spectrometer that performs digitization and analysis of 8 GHz bandwidth signals. This development is done in the framework of the NOEMA (Northern Extended Millimeter Array) project, which is a major upgrade of the IRAM Interferometer on the Plateau de Bure (France). The number of 15 meters antennas will be doubled from 6 to 12, the East-West baseline extended to 1.6 km, and the total IF bandwidth per receiver increased from 8 GHz to 32 GHz. This planned IF bandwidth comprises 4 IF bands of 8 GHz, since the receivers are implemented using an 8 GHz dual-polarization side-band separating (2SB) mixers.

After giving an overview of our spectrometer (Section 2), we describe in Section 3 the analog-to-digital conversion and the data synchronization with the FPGA. Also, we outline in Section 4 the signal processing architecture. Section 5 presents recent measurement results.

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2. SYSTEM OVERVIEW

The digital spectrometer is based on a prototype ADC from e2v working at 16 Giga samples per-second (Gsps) and an Altera Stratix IV GX FPGA (EP4SGX230KF40C3 device). This ADC is connected to the FPGA via 20 differential lines at a bit rate of 4 Gbps. To achieve a proper synchronization between both chips, the digitized data is scrambled before being transmitted using a pseudo-random binary sequence (PRBS). In addition, a pre-defined alignment pattern is sent during an initialization period.

Inside the FPGA logic, the data bits are aligned, descrambled and converted into two's complement format. This data is then filtered and demultiplexed into 64 overlapping sub-bands, which after selection are processed by pipeline FFT engines in order to reach high spectral resolution. Figure 1 presents the system block diagram of this spectrometer.

The spectrometer hardware is composed of two printed circuit boards (PCB). We first built a 10-layer PCB that integrates the ADC and the FPGA. The goal was to concentrate our design effort on the ADC-FPGA synchronization and the signal processing architecture. Later, a second board was built in order to include a broadband RF front-end, which performs both signal amplification and single-to-differential conversion. Figure 2 shows a picture of these boards.

In a future version of the system, both circuits will be integrated in a single board. Some additional parts will also be included to synchronize multiple boards, allowing to operate them in an interferometer system. Since RF and high-speed digital domains must co-exist, this board will be carefully designed in order to overcome several design challenges. Impedance matching over the 8 GHz input bandwidth must be achieved. The selected low-loss material must be compatible with the manufacturing constraints of the PCB stack-up. The complexity of the PCB can also increase due to the high routing density, pin count and supply current of the high-speed digital parts. Thermal considerations should be taken into account as well.

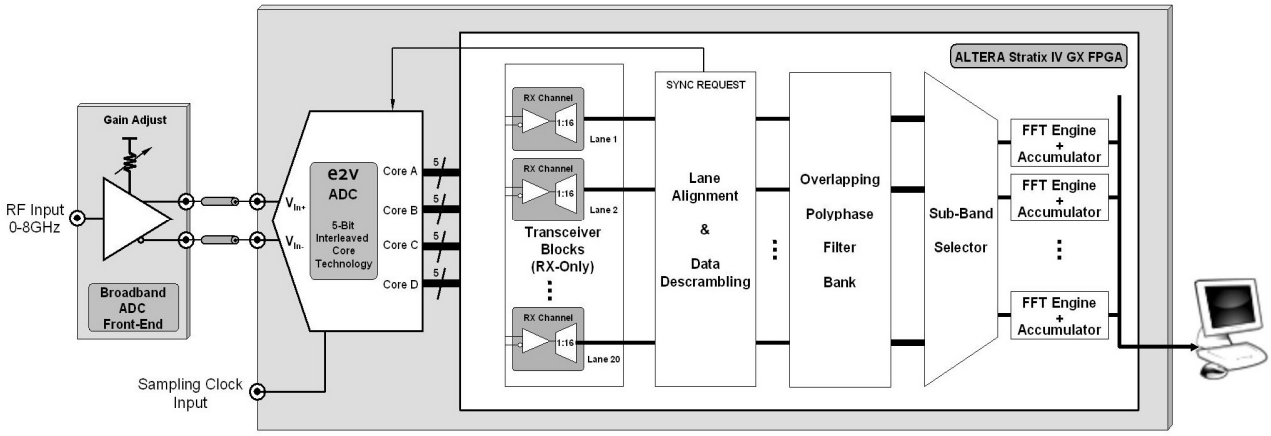


Figure 1. System block diagram.

3. ANALOG TO DIGITAL CONVERSION AND DATA SYNCHRONIZATION

3.1 E2V chip

We used an industrial prototype ADC chip provided by e2v[1]. This chip (EV5AS210) is a 5-bit resolution, 4-core time-interleaved ADC. It is specified to work up to 20 Gsps. However, as the full power input analog bandwidth (-3dB) of this ADC and the IF bandwidth of the NOEMA receivers are specified to 8 GHz, the sampling rate of our prototype was set to 16 Gsps.

The 5-bit 4-core ADC results in twenty 4-Gbps differential lines connected to the FPGA device, one for each output bit.

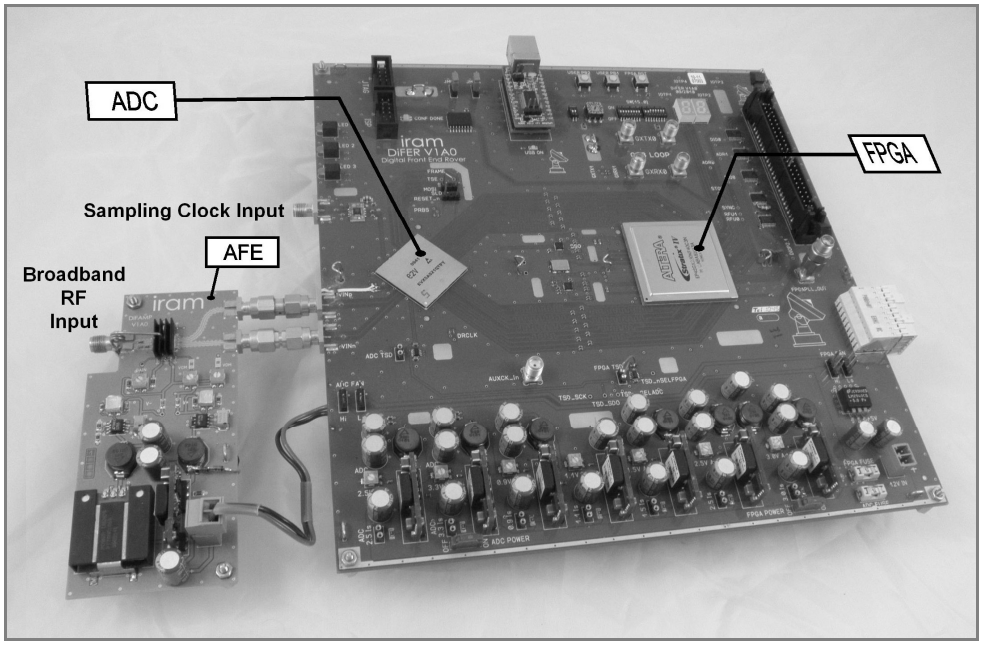


Figure 2. Picture of the spectrometer boards.

3.2 ADC-FPGA interconnection and data synchronization

Ensuring a reliable chip-to-chip data transmission at a high data rate of several Gbps is a technical challenge. As data rate increases, the classical "source synchronous" transmission scheme (data transmitted with its synchronous clock on a separate line) demands a very tight control on the PCB wiring and on the chip routing to minimize the length differences between the parallel data paths. This control is even more difficult if the data transmission must be performed between chips located on different boards in a larger system.

A different approach has been adopted by FPGA designers whose high-speed devices are often implemented in network switching systems, where data is transmitted in an asynchronous way (without any reference clock). To receive multiple asynchronous lanes at several Gbps, current FPGAs include embedded transceivers. A transceiver is a dedicated circuitry that includes configurable analog and digital blocks to implement standard and proprietary protocols operating from 600 Mbps up to 28 Gbps.

In our design, twenty 4-Gbps lines coming from the ADC are received by twenty FPGA transceivers. Each high-speed transceiver is composed of a clock and data recovery unit (CDR), a deserializer, a word aligner and a phase-compensation FIFO memory[2] (Figure 3).

To achieve a proper clock recovery by the CDR unit, the incoming data stream must contain frequent transitions. Otherwise a long stream of consecutive "0"s or "1"s transmitted by the ADC can produce a loss of synchronization of the CDR unit at the bit level. For this reason, the e2v ADC includes an internal PRBS generator that scrambles the digitized data before being transmitted to the FPGA. This PRBS generator uses a "$2^7 - 1$" polynomial. At the same time, this scrambling produces DC-balanced data streams. Therefore an AC-coupled transmission scheme can be implemented, allowing to interconnect ADCs and FPGAs whose differential ports have mismatching common-mode voltages.

Later, the deserializer converts the input serial stream into 16 parallel ones. The word aligner then aligns the received data using a known pattern hardwired into the ADC and sent during a synchronization procedure (initiated by request from the FPGA). This alignment pattern is simultaneously inserted into each data stream, which can therefore be transmitted through completely independent paths. On the receiver side, each word aligner seeks for this pattern that will serve as a timestamp for the later lane alignment.

Finally, the FIFO memory compensates the phase difference between each recovered parallel clocks and the FPGA fabric clock. This 250 MHz clock is a global clock distributed over the entire device and is the master clock for the later signal processing performed inside the FPGA logic.

Already in the internal programmable logic of the FPGA, a lane aligner module performs a global alignment to compensate the different latency between the 20 data flows coming from the transceivers. The aim is to provide a fully synchronized set of parallel data.

The data is then descrambled using the same PRBS sequence as the ADC, but regenerated inside the FPGA itself and initialized when the FPGA sends a synchronization request towards the ADC. A bit-reordering and a conversion to two's complement fixed-point format complete the data acquisition procedure. Thus, each 4ns, 64 samples of 5 bits are ready to be processed at the input of the polyphase filter bank.

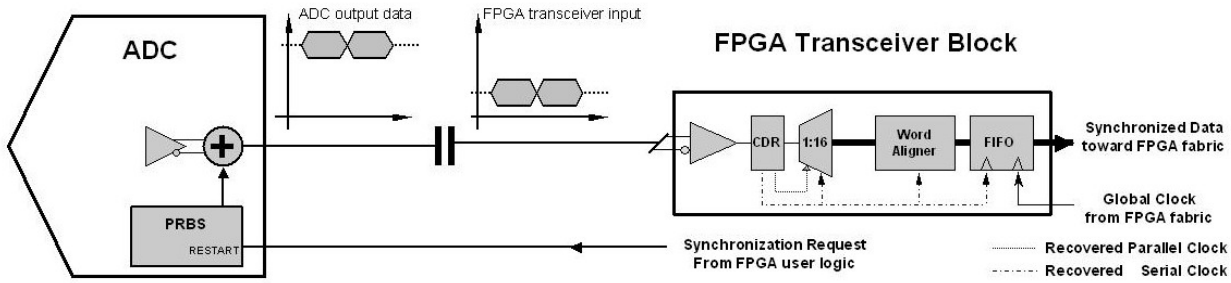


Figure 3. ADC-FPGA synchronization scheme for one differential line.

3.3 ADC calibration procedure

The ADC chip is implemented using a time-interleaved architecture in order to achieve the high sampling frequency of 16 Gsps. It integrates 4 fast ADC cores that work in parallel at a reduced sampling rate of 4 Gsps. The 4 cores convert the same input analog signal but taking samples shifted by one fourth of the effective sampling period. Thus, the interleaved ADC offers an aggregate sampling frequency that is 4 times higher than the individual core rate.

To obtain a good performance, the individual core responses must be as similar as possible. Otherwise the interleaved signal suffers from distortion which is traduced into undesired spurious components along its spectrum. To minimize these spurious components, the gain, the DC offset and the sampling delay of each ADC core must be adjusted by a calibration procedure. Then, the values for these parameters are written in specific digital registers of the ADC after power-up or a hardware reset. These registers are addressed via digital Serial Peripheral Interface (SPI).

Sinusoidal signals are usually used as test signals to calibrate interleaved ADC. However, by using Gaussian noise as test signals, we obtain cleaner spectra, reducing the complexity of the calibration procedure. Furthermore, Gaussian noise signals emulate radio-astronomical signals and permit to test the ADC under more realistic conditions.

Thus, the calibration procedure is based on the estimation of the statistics and the power spectrum from records of consecutive digital samples coming from every ADC core. This estimation is performed by computer software. The samples are transmitted from the FPGA to the computer via an USB interface.

By estimating the variance and the mean of the sample records, the gain and DC offset parameters are calculated. These parameters are tuned until the statistical estimates are as similar as possible between the different ADC cores. As the time-interleaving must be adjusted over the entire frequency band, wideband Gaussian noise (from DC to 8 GHz) is used as test signal.

To tune the delay parameters, we used a band-pass filtered Gaussian noise. To achieve more accuracy, the center frequency of the band-pass filter must be as high as possible, close the Nyquist frequency. Then a spectral analysis of the interleaved response is calculated, and the delay is tuned to minimize the spurious images that appear due to the phase mismatch.

4. DIGITAL SIGNAL PROCESSING

4.1 Overlapping polyphase filter bank

We designed a polyphase multirate filter bank (or channelizer) that separates the digitized real signal of 8 GHz bandwidth into 64 complex sub-bands. These output sub-bands are complex-valued baseband signals and have a bandwidth of 250 MHz each.

A polyphase filter bank (PFB) is a very efficient implementation of a uniform multirate filter bank using a Fast Fourier Transform (FFT)[3,4]. A classical uniform multirate filter bank is an array of digital baseband down converters with equally-spaced center frequencies and identical bandwidth (Figure 4(a)). Each down converter performs a frequency down conversion, shifting the sub-band of interest to baseband; a low-pass filtering to select this sub-band and a down-sampling to reduce the sampling frequency but maintaining the Nyquist-Shannon theorem. The sampling frequency is reduced by a factor equal to the number of channels of the multirate filter bank. Since 250 MHz is a feasible rate for the FPGA logic, 64 is the number of channels chosen for our filter bank.

Figure 4(b) shows the block diagram of a standard 64-channel polyphase filter bank. The digitized input signal is first demultiplexed by a factor of 64, represented by a commutator in the figure. This commutator is followed by an array of digital filters, which are decimated-by-64 versions of the original low-pass filter used in the equivalent uniform multirate filter bank. This means that the original FIR low-pass filter of *N* coefficients is partitioned into 64 all-pass FIR polyphase filters of *N*/64 coefficients. These filters are known as polyphase filters because they present different linear phase responses. Finally, the filtered signals are processed via a parallel FFT engine to obtain the output sub-bands.

This polyphase architecture offers increased efficiency in both speed and area, which are key aspects for programmable systems based on FPGAs. Note the logic saving due to the polyphase partition in the filtering stage and the computational efficiency of the FFT algorithm. In addition, all the data processing is performed at the reduced sampling rate. Because of all these benefits, the polyphase digital filter banks are well suited for being the first processing stage of a digital spectrometer or correlator. This first processing stage is generally known as digital receiver.

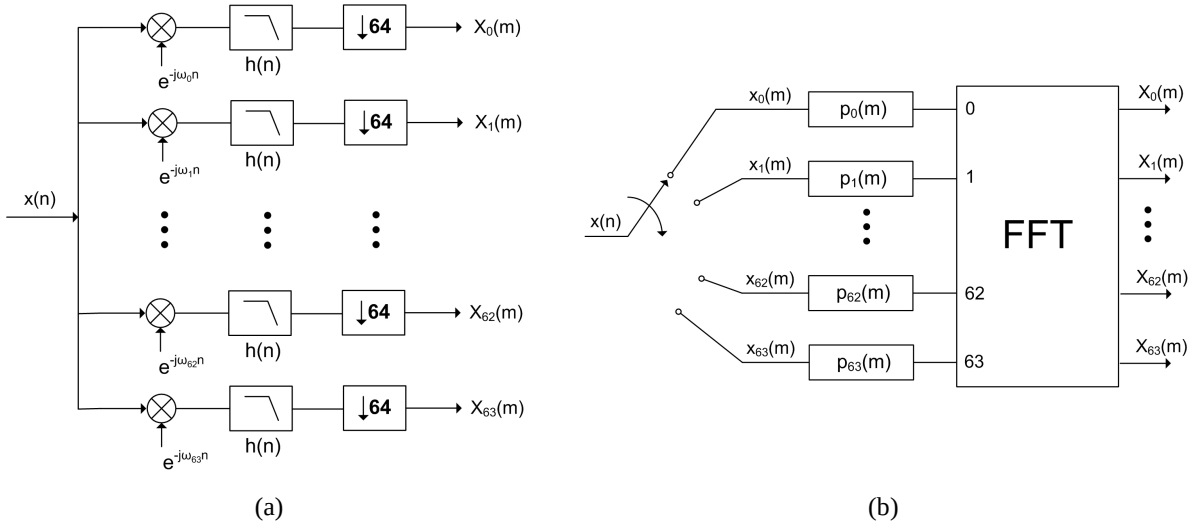


Figure 4. (a) Classical 64-channel uniform multirate filter bank. (b) Equivalent efficient polyphase representation.

In radio-astronomy observations, the goal is to obtain continuous spectral information over a wide bandwidth. However, the spectral response of the standard polyphase filter banks presents discontinuities at the edges of the sub-bands (Figure 5). To overcome this drawback, a 50% overlapping version[5,6] of the polyphase filter bank is implemented.

This overlapping polyphase filter bank (OvPFB) can be considered as two polyphase filter banks whose center frequencies are shifted by half of the channel bandwidth (Fig. 5). The first filter bank is a standard polyphase filter bank

(as described above), whose first sub-band is centered at the zero frequency (known as even type channel stacking arrangement). The second filter bank is a polyphase filter bank based on an odd Fast Fourier Transform, where the first channel is centered at a frequency equal to half the channel spacing (odd type channel stacking arrangement).

A careful design of this overlapping version permits to reduce the logical resources used. In fact, these two filter banks can share the multipliers in the filtering stage, as their coefficients have the same absolute value. Furthermore, the required number of filter coefficients is reduced since, due to the overlapping approach, the specifications of the prototype filter are less stringent. As the input digitized signal is real-valued, symmetry properties can be applied in order to use a single parallel FFT. This single FFT works on complex-valued input samples that are obtained via arithmetic operations over the real-valued samples coming from the filtering stage. For our design, this complex FFT is implemented using a radix-4, decimation-in-frequency (DIF) fully-parallel architecture.

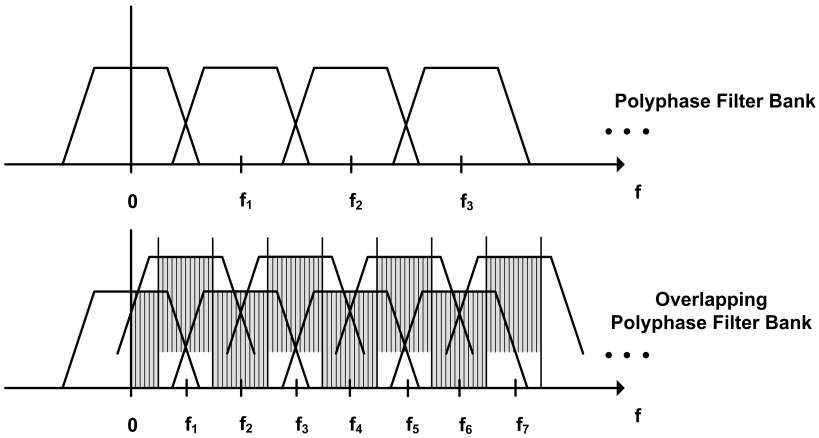


Figure 5. Overlapping filter bank concept, implemented to obtain continuous spectral information.

4.2 High resolution spectral analysis

Following the digital filter bank, FFT engines are used to perform a high resolution spectral analysis. Each FFT engine processes a 250-MHz complex-valued signal corresponding to an output sub-band of the OvPFB. For continuum or extragalatic millimeter-wave astronomy, resolutions of a few megahertz are often required. Instead, higher resolutions up to a few tens of kilohertz are demanded for galactic observations, where extremely narrow lines must be resolved. Present back-ends must therefore provide spectral flexibility.

This flexibility was obtained by using two different types of FFT engines. In our design, 128-point FFTs were used to achieve a low spectral resolution (~ 2 MHz of channel spacing), and 4096-point FFTs to obtain a high resolution of 50 kHz.

A full spectral coverage (64 sub-bands analyzed) could not be achieved due to a limitation in the logic resources of the selected FPGA device. For this reason, a maximum number of 32 FFT engines of 128 points or a maximum of 16 FFTs of 4096 points could be implemented. However, FPGA devices doubling the number of logic elements are already available, at the expense of an additional cost.

We are currently designing a future back-end, based on this prototype, to provide an entire spectral analysis at a low frequency resolution and to offer a finite number of “zoom windows” or sub-bands analyzed at high resolution. In our opinion, a ratio of 1/4 should be a good compromise. If better spectral resolution is demanded, FFTs with a higher number of points could be utilized, but decreasing the number of available zoom windows.

Figure 6 shows the block diagram of the signal processing pipeline applied to one complex-valued sub-band coming from the filter bank. A FFT engine, preceded by a programmable windowing operation, transforms the sub-band to the frequency domain. This FFT engine is based on the FFT MegaCore Function, which is a highly-parametrizable FFT processor developed by Altera[7]. The FFT MegaCore Function uses a radix-2^2 pipelined architecture, whose butterfly structure is the same of the radix-2 architecture, but the multiplicative complexity is equivalent to a radix-4 architecture[8].

The FFT engine is followed by a frequency clipping module, which discards half of the frequency bins or channels computed by the FFT. These discarded bins are the ones that are close to the sub-band edges. Note that due to the 50% overlapping approach, only the central region of the sub-band around the zero-frequency must be preserved to obtain a perfect frequency stitching. Thereby, the following blocks process only useful data and the clock frequency can be halved, optimizing the power consumption. Finally, the squared absolute value of this clipped spectrum is computed to obtain the power spectrum. Then, successive power spectra are averaged via a synchronous accumulator based on a RAM memory. This accumulation reduces the system noise fluctuations, improving the detection of weak astronomical signals.

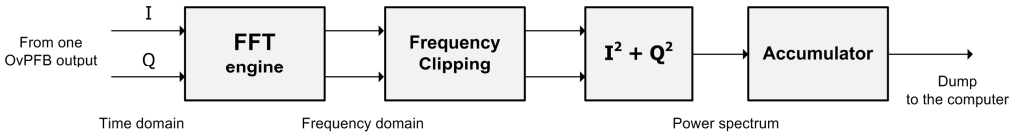
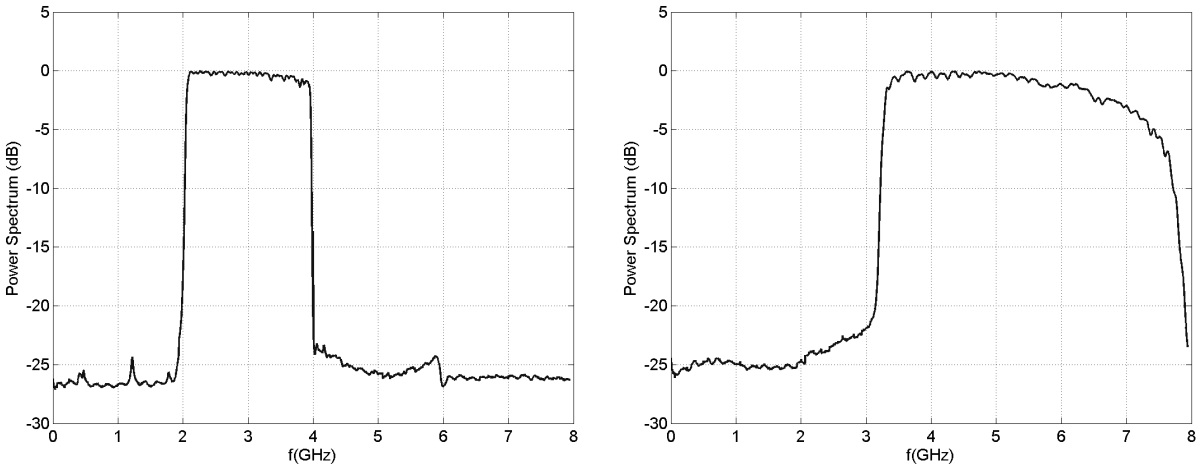


Figure 6. Signal processing architecture to analyze one overlapping sub-band at a high spectral resolution (from a few MHz up to a few tens of kHz).

5. RESULTS

The spectrometer was tested in the laboratory in order to evaluate its performance. Figure 7 shows two examples of measured spectrum at a resolution of approximately 2 MHz, for a total 4065 frequency points (the first sub-band is real-valued and its spectrum is therefore symmetric -Figure 5-). 128-point FFT engines were utilized to analyze the overlapping sub-bands. Each spectrum was generated from two consecutive measurements in order to cover the entire input bandwidth.

The integration time is 33.55 ms, which corresponds to 65536 FFTs accumulated for each sub-band. The test signals are filtered Gaussian noise. For the spectrum in Fig. 7.(a), a 2-4 GHz band-pass filter was used. This is the digitizer filter for the current IRAM and ALMA correlators. For the plot in Fig. 7(b), a 3.5-7.5 GHz band-pass filter was utilized. This plot shows the ADC roll-off at high frequencies (close to 8 GHz).



(a) (b)

Figure 7. Measured spectra for filtered Gaussian noise signals. (a) 2-4 GHz band-pass filter. (b) 3.5-7.5 GHz band-pass filter.

6. CONCLUSIONS

We have outlined the design and presented some results of a digital spectrometer that addresses the present-day demands on analysis of broadband signals at a flexible range of spectral resolutions. This spectrometer can digitize signals of an instantaneous bandwidth 4 times wider than the latest generation of digital back-ends currently in service at IRAM or ALMA. It is characterized by a uniform and continuous spectral response and also can achieve high spectral resolutions up to a few tens of kHz. With a speed of 16 Gsps, this design is an interesting step in the development of digital spectrometers for radio-astronomy.

The purpose of this work was to acquire experience on recent digital technology, in view of the design of a new correlator for the coming upgrade of the IRAM Plateau de Bure interferometer (NOEMA project). This future correlator, whose digitizer board will be largely inspired from the spectrometer described here, will include 96 such devices, plus the corresponding baseline processing.

REFERENCES

[1] e2V. Broadband Data Converters. http://www.e2v.com/products-and-services/hi-rel-semiconductor-solutions/broadband-data-converters/

[2] Altera Corporation. “Transceiver Architecture in Stratix IV Devices”. Stratix IV Device Handbook Volume 2: Transceivers. (December 2011). http://www.altera.com/literature/hb/stratix-iv/stx4_siv52001.pdf

[3] Crochiere, R. and Rabiner L., [Multirate Signal Processing], Prentice-Hall Inc., Upper Saddle River, NJ, 289-326 (1983).

[4] Harris, F. J., [Multirate Signal Processing for Communication Systems], Prentice-Hall PTR, Upper Saddle River, NJ, 127-143 (2004).

[5] Wilson, W. E., Ferris, R. H. et al, “The Australia Telescope Compact Array Broadband Backend (CABB): Description & First Results,” Monthly Notices of the Royal Astronomical Society 416, 832-856 (2011).

[6] Comoretto, G., Melis, A., Tuccari, G. “A wideband multirate FFT spectrometer with highly uniform response,” Experimental Astronomy 31, 59-68 (2011).

[7] Altera Corporation. “FFT MegaCore Function. User Guide”. (November 2011). http://www.altera.com/literature/ug/ug_fft.pdf

[8] He S. and Torkelson M., "A New Approach to Pipeline FFT Processor," Proc. 10th International Parallel Processing Symposium (IPPS '96), 766-770 (1996).