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VME board AXPOS

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Keywords:

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Change Record

REVISION	DATE	AUTHOR	SECTION/PAGE AFFECTED	REMARKS

Content

1 AXPOS VME Board:

1.1 Description:

This board allows reading the Antenna position in 1/10th of an arc-second units , as a 32-bit word. Using 32 bits , the entire rotation range of the antenna (+/- 270 deg) can be used without any further sign bit.
The data is encoded in standard signed binary .
The module is completely self-contained , and needs no external reference signal. All clocks are derived from the VME System Clock.
The heart of the module is a complex quadrature mixer and a numerical PLL which does not use any frequency translation .

For easy maintenance :

There is no adjustment on the board .
Test points are accessible on front-panel for checking the input signal without removing the board from the crate.
The detailed status of the board is readable on front-panel leds , allowing to know exactly what's going on.
A "TEST" mode is implemented on the board , which allows a simple check with a scope , on 2 test points.

WHAT THIS MODULE DOES :
Convert the Sine/Cosine signal of the encoder into a 32 bit POSITION word.
Preload this word with required value in a synchronous (using encoder REF pulse) or asynchronous way
Handle a status register , and generate interrupts (to the uP) upon events.

WHAT IT DOES NOT DO :
It does not correct the errors of the encoder signals,
It does not extrapolate any velocity information from these signals.

1.2 Registers :

All registers of the board are accessible in Standard Mode (Address on 24 bits).
Address Modifier = 39 or 3D.

Position Register POSR , 32 bit read-only : position in 1/10 arc-second.
Accessible in Longword access at Board-Address + 0

Preload Register PLDR , 32 bit write-only : same convention .
Accessible in Longword access at Board-Address + 0

Status Register STSR , 8 bit read-only.
Accessible in Byte access at Board-Address + 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TEST	UNLOCK	LAMP	SIGNAL	APDONE	SPDONE	REF	SPE

TEST = The board is in TEST mode (switch K2 on the board is OPEN).

UNLOCK = set upon detection of a PLL lockout.

reset by (RESET + STARTUP + (A)PRELOAD REQUEST)

LAMP = Encoder current is too weak : probably a Lamp failure .
reset when (Status read AND Lamp OK).

SIGNAL = Encoder signal out of tolerance (5 V Peak +/- 10%).
This check effectively controls that (SIN**2 + COS**2 = 1).
reset when (Status read AND Signal OK).

APDONE = ASYNCHRONOUS PRELOAD done.
reset by (RESET + STARTUP + (A)PRELOAD REQUEST)

SPDONE = SYNCHRONOUS PRELOAD done.
reset by (RESET + STARTUP + (A)PRELOAD REQUEST)

SPE = SYNCHRONOUS PRELOAD required , waiting Encoder REF pulse.
reset by (REF + RESET + STARTUP + APRELOAD REQUEST + SPDONE)

REF = set upon detection of reference pulse during SYNCHRONOUS PRELOAD.
reset by (RESET + STARTUP + SPDONE)
CAUTION : this bit does NOT reflect the STATE of the encoder Reference ,
as displayed on Front-Panel Led "REF".

Command Register CMDR :

2-bit write-only *virtual* register using D0, D1 (LSBits of the VME data Bus) .
Accessible in Byte access at Board-Address + 1

D1	0	1	1
D0	1	0	1
FUNCTION	Asynchron Preload	Synchron preload	Total Reset

RESET function :
The VME controller "RESET" is done when (Startup + VME Sysreset).
The complete Board "RESET" is done when (Startup + VME RESET Command).
In order not to loose the initialisation of the antenna , the position register is not reset by " VME SYSRESET " .

1.3 Interrupts

IT “Error “ is generated upon "UNLOCK" rising edge .
The equation of IT “Error”: may be modified (see GAL CODSTS) in order to generate it upon other events .
CAUTION : TEST mode will assert UNLOCK and thus IT “Error”.

IT “Done” is generated upon APDONE rising edge or SPDONE rising edge.

IT “Error” has highest priority .
Both interrupts share the same IRQ level, but each interrupt uses its own dedicated vector.

1.3.1 Vectors:

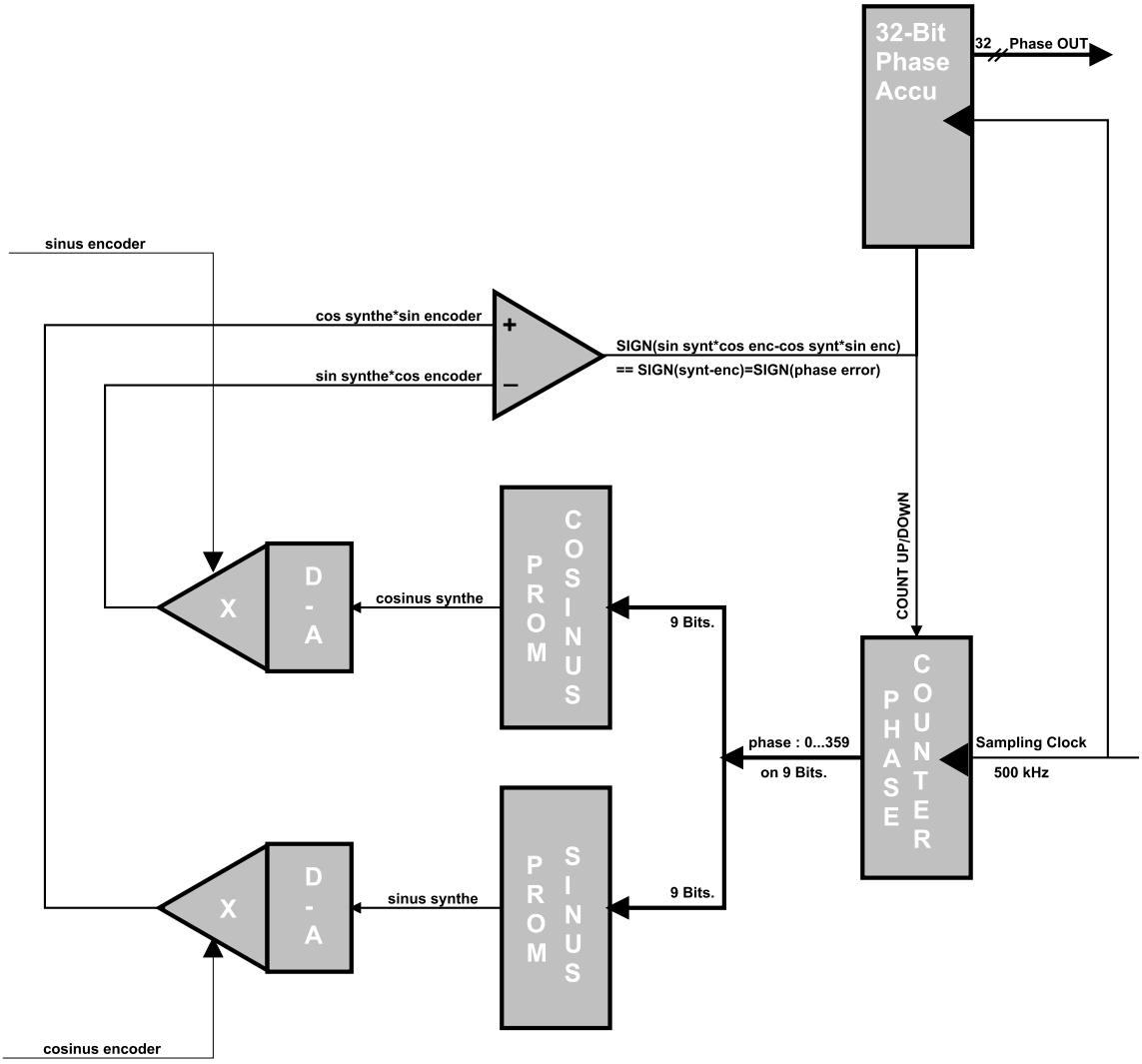
The Vector Base value is selectable, using the on-board switch RC1.

Switch Position	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Vector Base	F0	E0	D0	C0	B0	A0	90	80	70	60	50	40	30	20	10	0

-Vector “Error” = Vector Base + 2.
-Vector “Done” = Vector base + 0.

1.4 Performances

The encoder signals: A complete period of the encoder signal corresponds to a 36 arc-second rotation of the antenna axis. The Axpos board interpolates the encoder signals , and the interpolation factor is 360. This means that the measured position increment will be 0.1 arc-second.
The numerical PLL samples the position with a 500 kHz rate , and each sampling results in a correction of +/- 0.1 arc-sec of the measured position.



POSITION PLL Block diagram

PLL velocity:
The maximum antenna velocity the PLL can follow is :
(500 * 10E3 * 0.1) arc-second/second
= 14 deg/second .
This possibility far exceeds the maximum speed of the antenna (1 deg/sec) and thus allows a very good insensitivity to short duration accelerations. As this system is not linear, it is not easy to define criteria as Loop Bandwith or Damping factor .

The only predictible parameter is the Slew-Rate : 14 deg/sec .
This also means that the phase-lock is always possible on any frequency which is less than 14 deg/sec , the final error being +/- 0.1 arc-sec .

EXAMPLE :
If we assume an initial pointing error of 10 arc-sec , and an antenna speed of 1 deg/sec , the phase-lock time will be = 10 / [(14 - 1) * 3600] seconds, and the final (+/- 0.1 arc-sec) value will be reached within 214 microseconds.

The PLL Lockout detection is reliable , as it measures in real-time the phase shift between the input signal and the synthesized signal , and trigs when this phase shift exceeds +/- 178 degrees (== transient 17.8 arc-second antenna pointing error).
This limit value is related to the transfer function of the phase comparator , whose output = SINUS (PHI SYNTHE - PHI ENCODER). As this is not a sequential phase comparator , it is not able to track out of the range [-PI..+PI] .
The main advantage of such a phase comparator is its good insensitivity to noise , especially to glitches which would generate a phase-jump of 36 arc-sec, if using a sequential phase comparator which locks over the range [-2*PI..+2*PI].

1.5 Electrical requirements:

As this is a 32-bit module , it requires a complete P1-P2 VME backplane , with P2 connectors being VME-compliant on row B.
THE BOARD HAS NO CONNECTION ON ROWS A AND C OF P2.

POWER : The Board needs VME standard voltages :
+ 5V , 1.5 A
+ 12V , 0.1 A
- 12V , 0.1 A

1.6 Switches:

RC1 : Vector Base selection.

RC4 : Board Address bits 8..11
RC3 : Board Address bits 12..15
RC2 : Board Address bits 16..19
RC5 : Board Address bits 20..23

K1: Switch “Wave select”.
When installed , K1 selects Sine/Cosine lookup table of the Proms. When removed , the Proms supply wave forms similar to the encoder signals (if previously stored inside the Proms).

K2: Switch “Test”.
Whit K2 installed , the board is in normal operating mode.
Whith K2 removed, the board is in Test mode. In that case , sine waves should be observed on test points TP1 and TP2 .
These sine waves normally have an amplitude of 5 Volt peak , a frequency of 1.389 kHz , and a phase shift of Pi/2. The observation of these signals guarantees that the quadrature mixer works fine.
When the board is in TEST mode , red LED "TST" on the front-panel blinks , red LEDs "SIG" and "UNL" are lit, and IT "ERROR" is set, which is normal.

1.7 Front-Panel (from top to bottom):

Vector display : The encoder phase modulo 36" is displayed as a rotating segment with a step of 6"(6.4" exactly).This really helps when the antenna is tracking .
Led R/W (yellow) flashes any time the board is accessed through the Bus.
Led INT (red) turns on when the board generates a VME interrupt , and off when this interrupt is acknowledged .
Led UP and **Led DOWN** (yellow) reflect the sign of the velocity of the antenna.

Led REF (red) is lit when the Reference Pulse of the encoder is ON.
Led SPE (blue) turns on when a synchronous preload has been required ,
and off when the synchronous preload is done (after "REF" has been detected).
Led SPD (green) turns on when Synchronous Preload is done ,
and is reset upon ((A)Preload request + PLL Unlock).
Led APD (green) turns on when Asynchronous Preload is done ,
and is reset upon ((A)Preload request + PLL Unlock).
Led SIG (red) turns on when the signal from the encoder is inconsistent.
The board continuously checks that (SIN**2 + COS**2 = "1" = 5V +/- 10%).
Led LPF (red) turns on when the signal "L" from the encoder is on , thus
indicating that the encoder current is too weak (e.g. lamp burnt).
Led UNL (red) turns on when a PLL Lockout has been detected.This generally
happens if the angular velocity of the encoder axis exceeds 14 deg/sec.
Led UNL is reset upon next (A)synchronous Preload.
Led TST (blinking red) blinks when the board is in Test mode.
In that case , SIG and UNL should turn on.

UNDER NORMAL CIRCUMSTANCES , NO RED LED SHOULD STAY ON .

CONNECTOR **J1** : Encoder Sine Test Point, SMB connector.

CONNECTOR **J2** : Encoder Cosine Test Point, SMB connector.

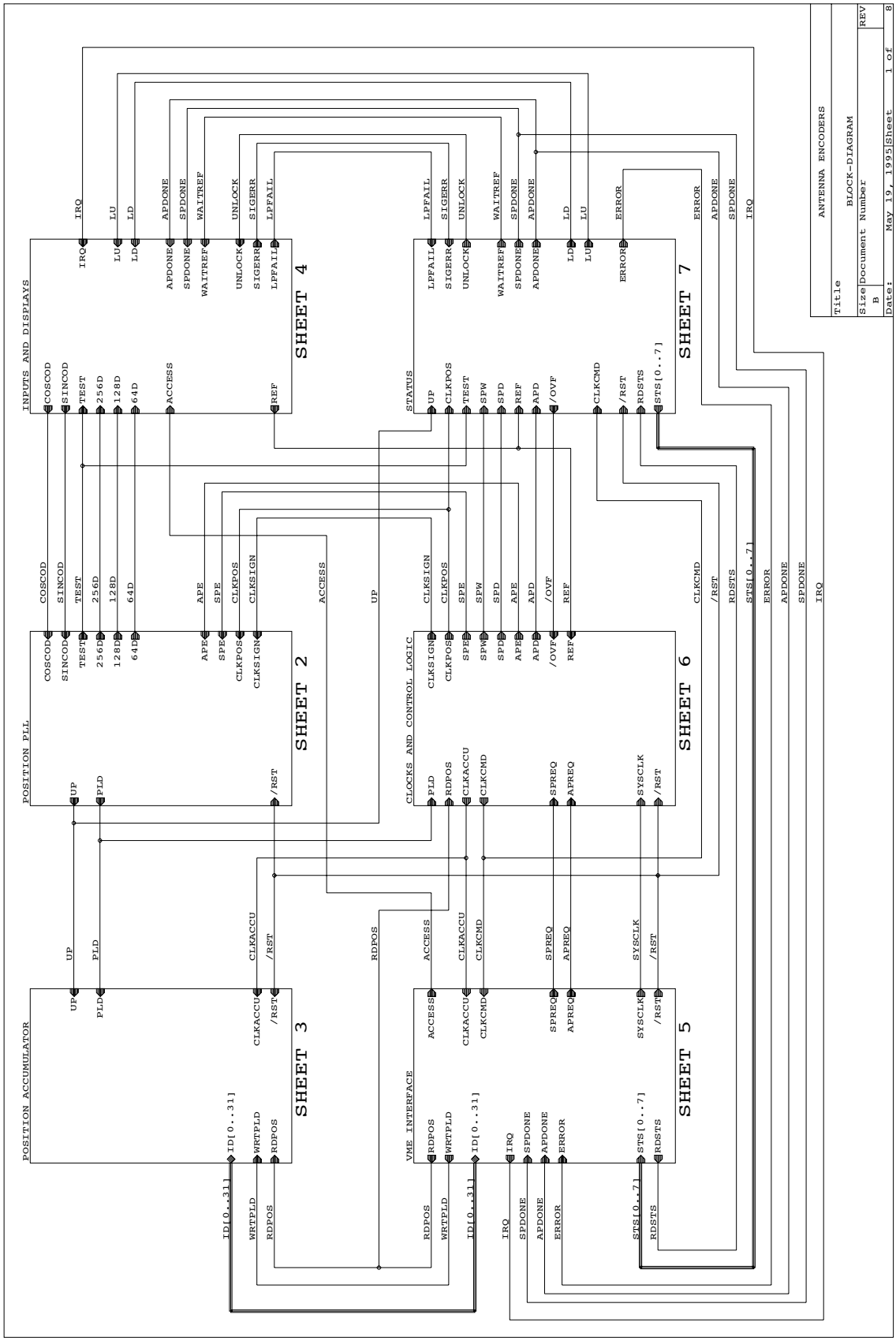
CONNECTOR **J3** : Encoder Ref Test Point, SMB connector.

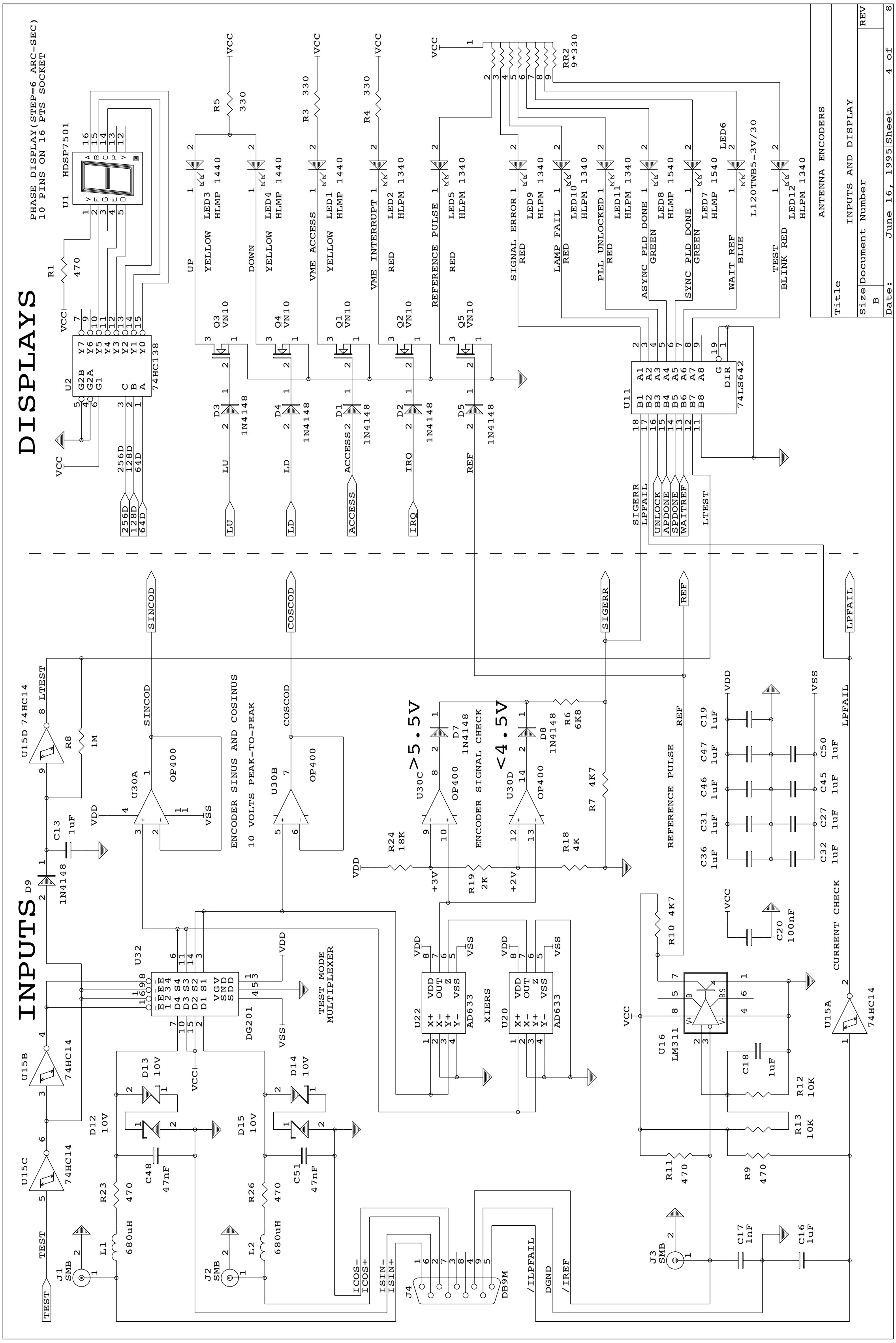
CONNECTOR **J4** : Encoder inputs , this is a DB9 Male connector .

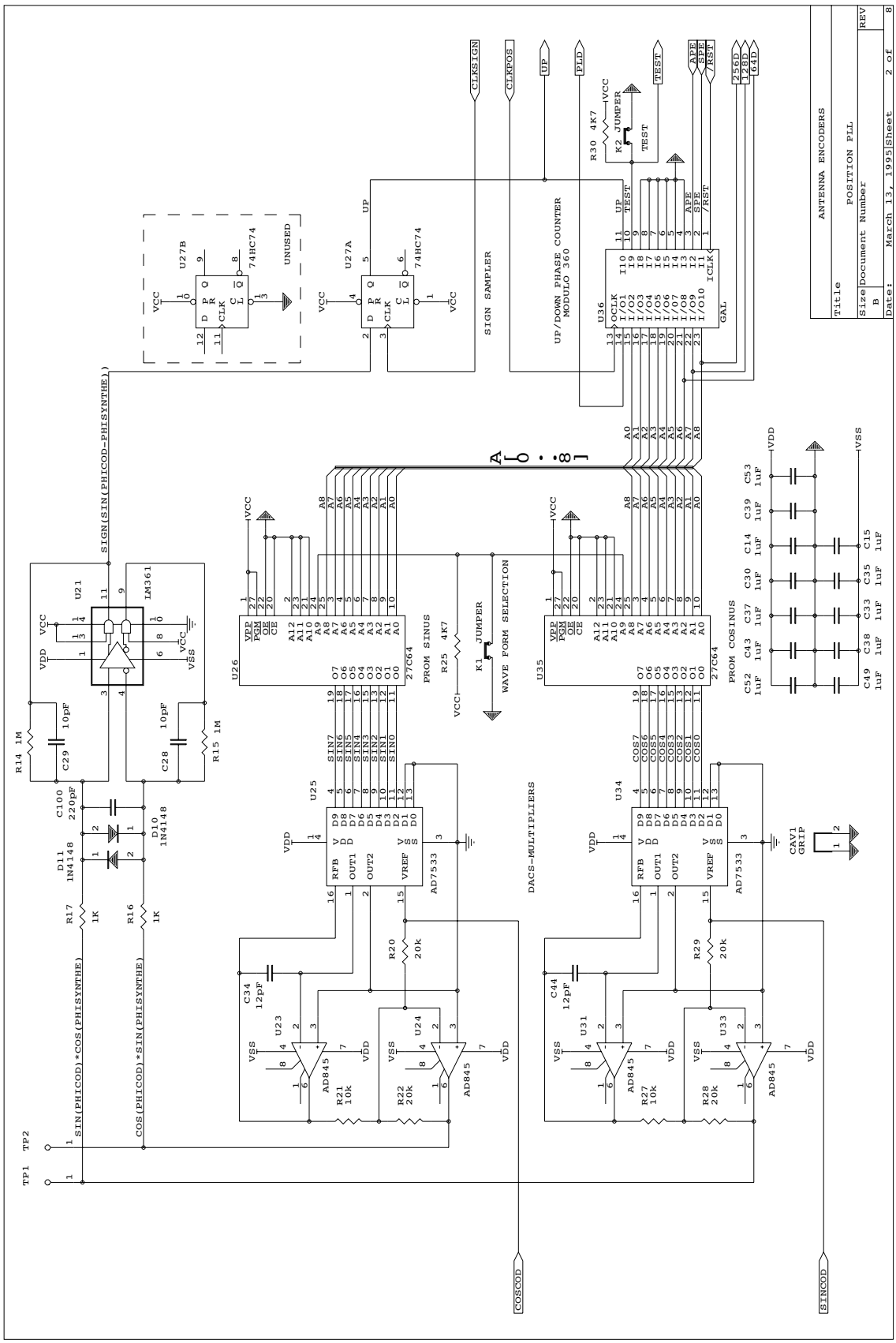
1.7.1 J4 pinout:

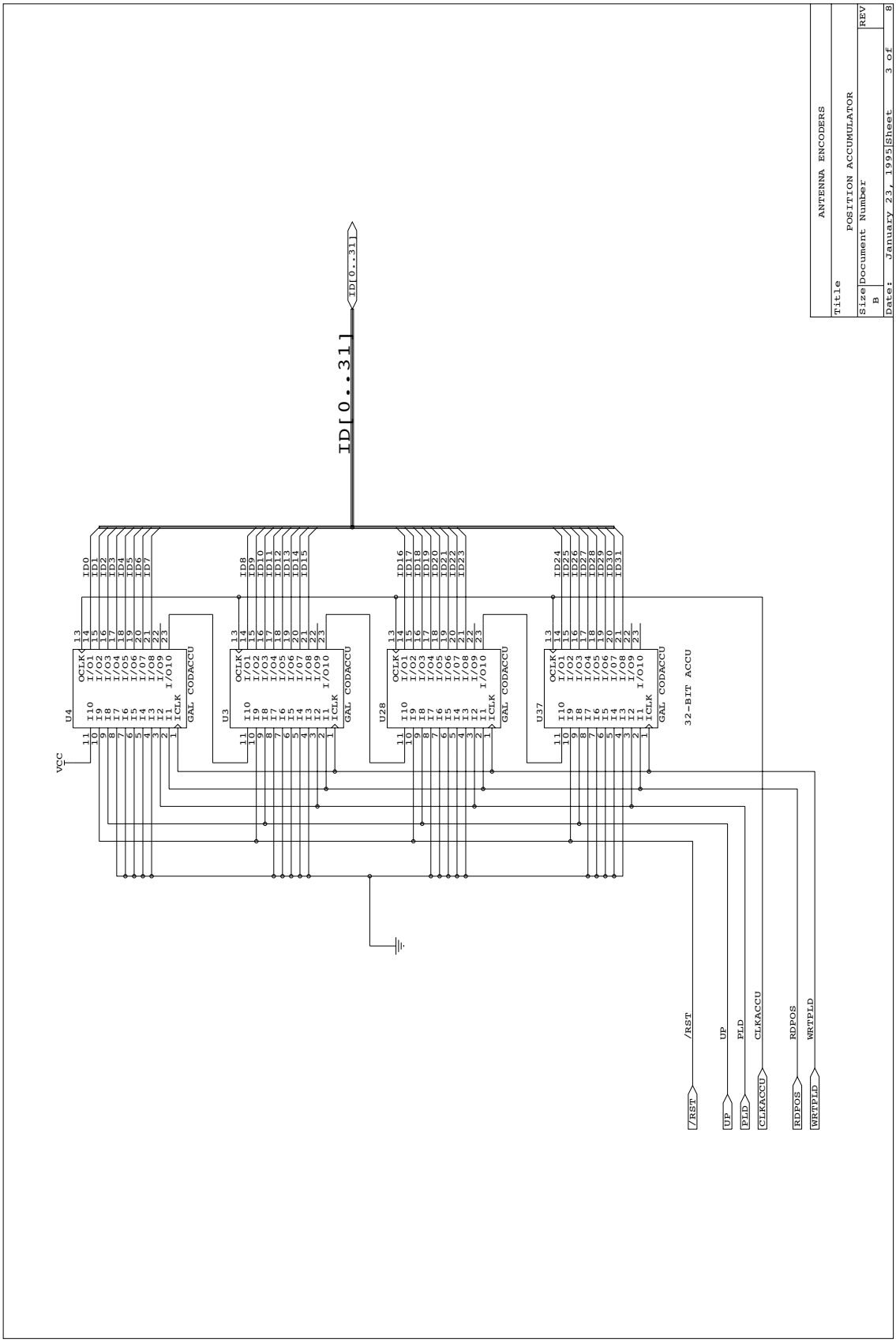
1	Encoder SINE signal
2	Encoder COSINE signal
3	unused
4	Encoder REF signal
5	Encoder LAMP signal
6	Analog GND
7	Analog GND
8	unused
9	Digital GND (connected to Analog GND on the board)

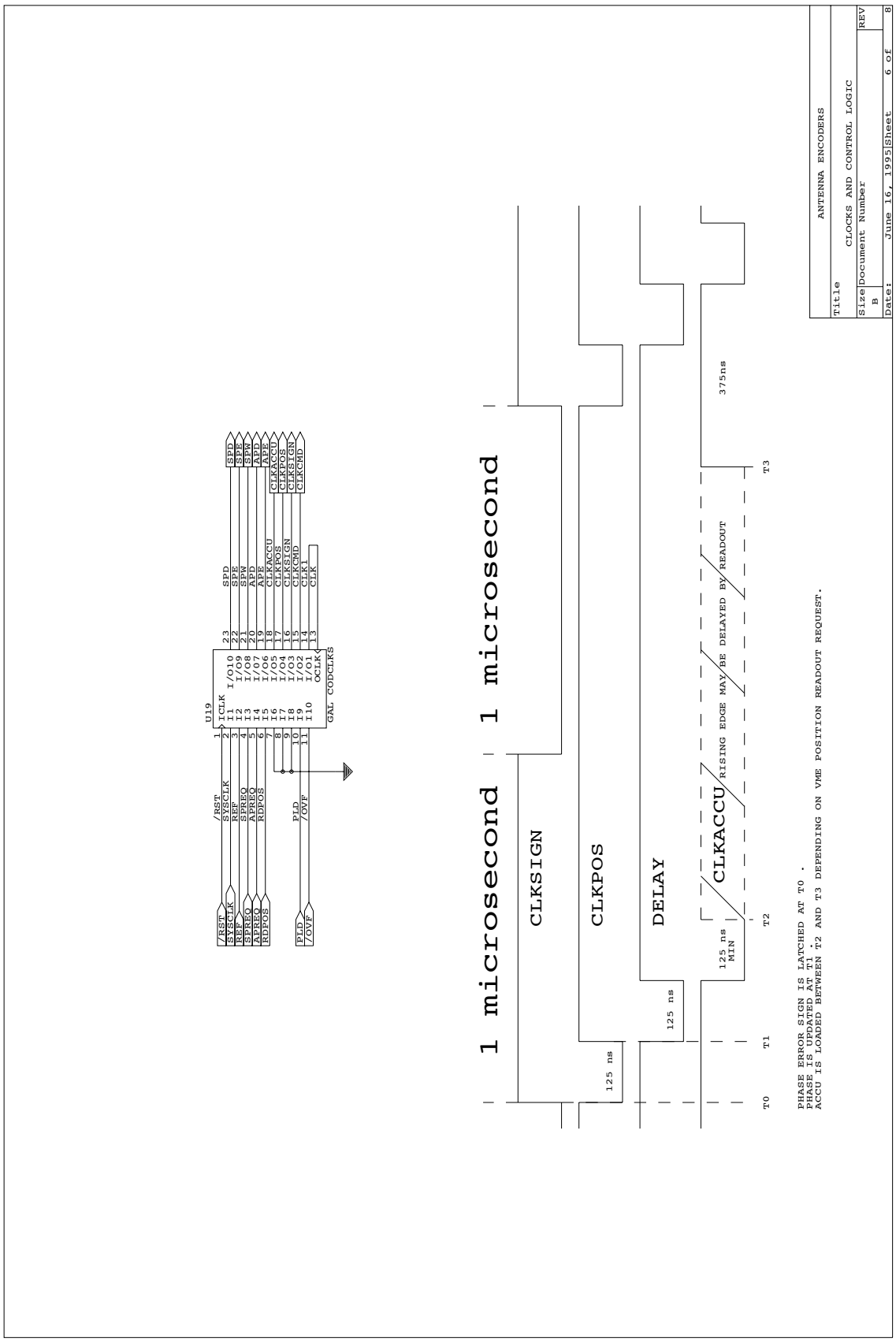
1.8 AXPOS Schematics:

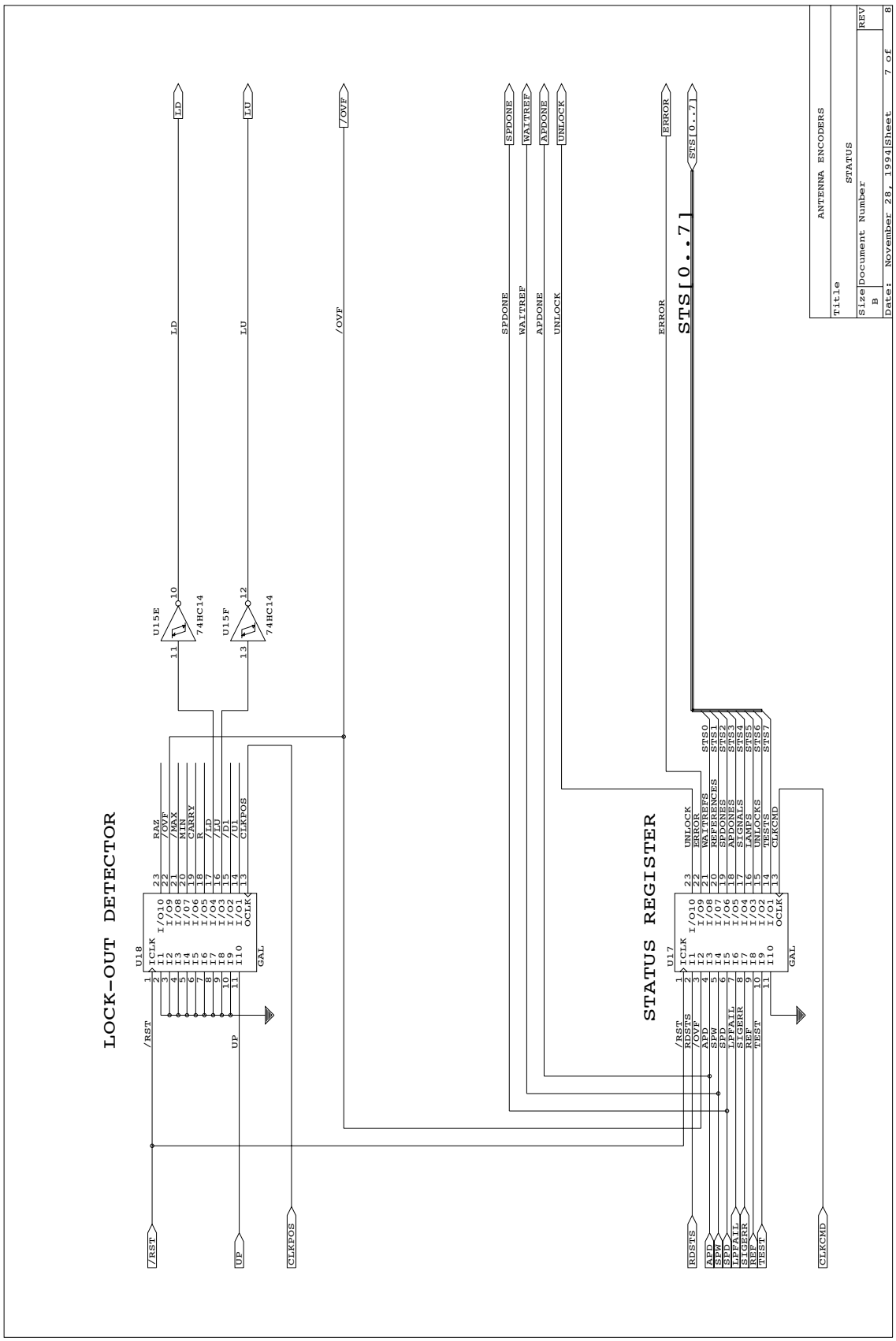


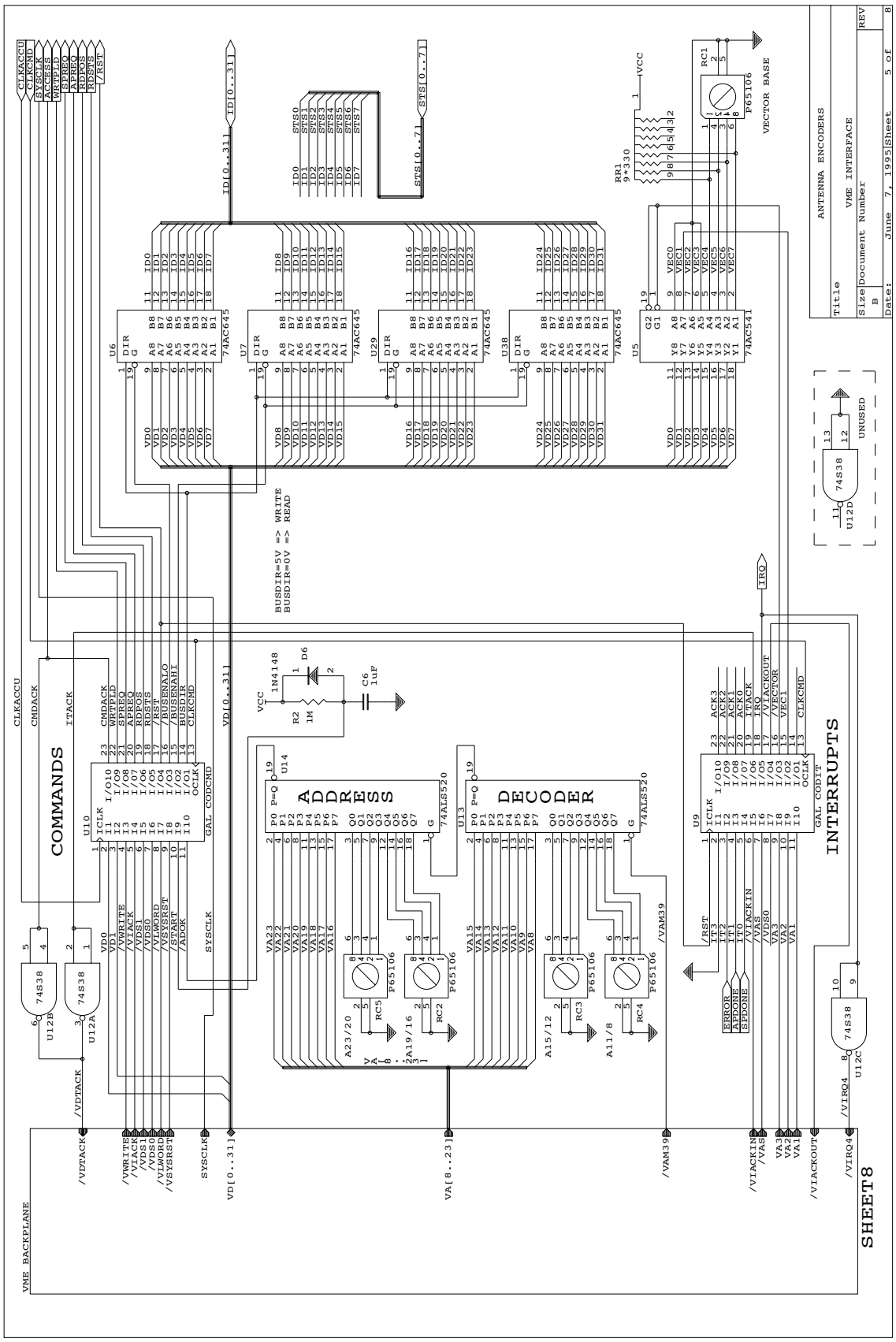

DISPLAYS
INPUTS
ANTENNA ENCODERS
Title
INPUTS AND DISPLAY
Size Document Number
B
REV
Date: June 16, 1995 Sheet 4 of 8

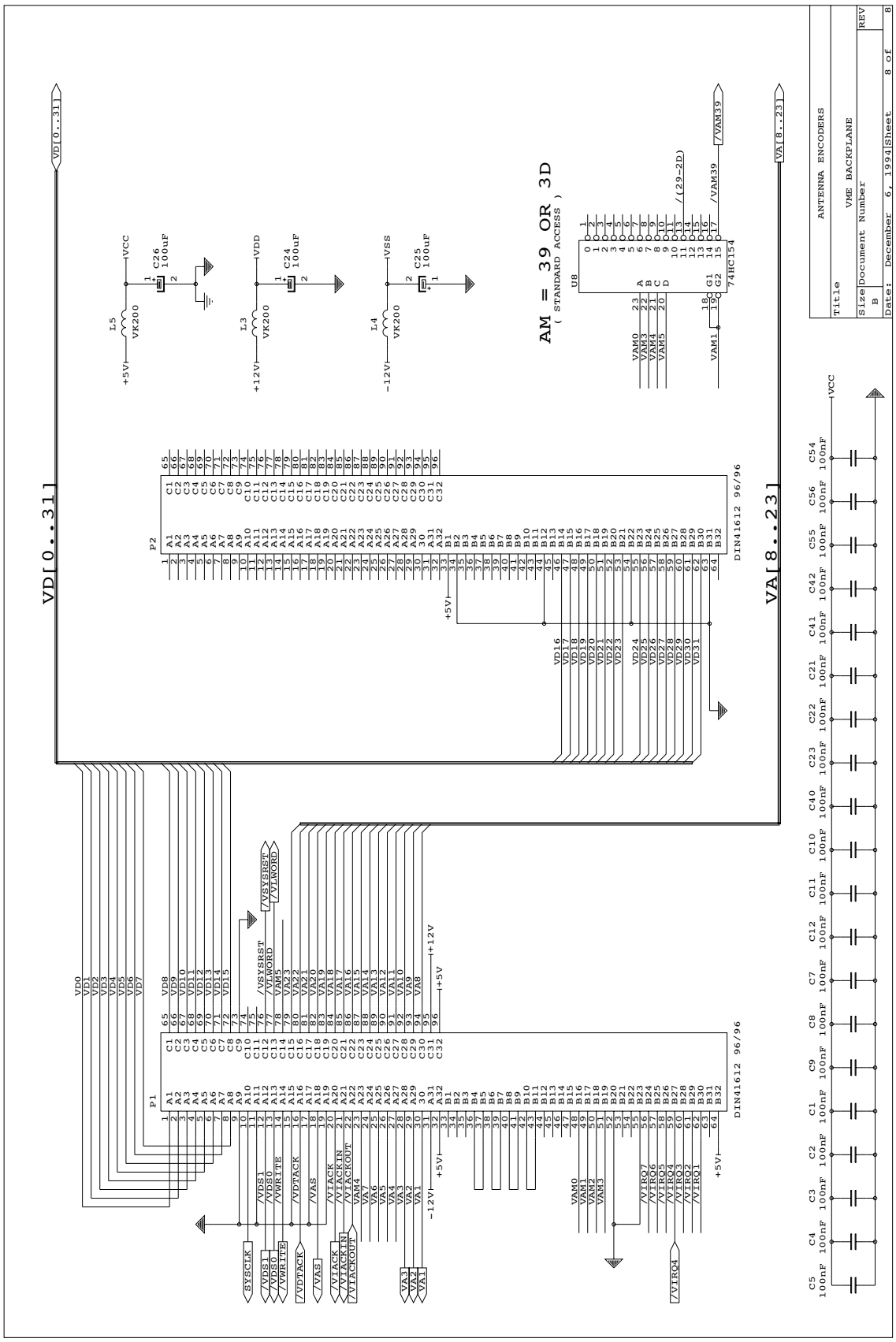

ANTENNA ENCODERS
POSITION PLL
Document Number
March 13, 1995
Sheet 2 of 8
SIGN SAMPLER
UP/DOWN PHASE COUNTER MODULO 360
PROM SINUS
PROM COSINUS
WAVE FORM SELECTION
DACS-MULTIPLIERS
SIN(PHICOD)*COS(PHISYNTHE)
COS(PHICOD)*SIN(PHISYNTHE)
SIGN(SIN(PHICOD-PHISYNTHE))
COSCOD
SINCOD
CLKSIGN
CLKPOS
UP
PLD
TEST
APE
SPE
/RST
256D
128D
64D
VCC
VDD
VSS


ANTENNA ENCODERS
Title
POSITION ACCUMULATOR
Size B
Document Number
REV
Date: January 23, 1995
Sheet 3 of 8
ID[0..31]
U4
U3
U28
U37
GAL CODACCU
32-BIT ACCU
VCC
/RST
UP
PLD
CLKACCU
RDPOS
WRTPLD


U19
GAL CODCLKS
/RST
SYSCLK
REF
SPREQ
APREQ
RDPOS
PLD
/OVF
SPD
SPE
SPW
APD
APE
CLKACCU
CLKPOS
CLKSIGN
CLKCMD
CLK1
CLK
OCLK
1 microsecond
1 microsecond
CLKSIGN
CLKPOS
DELAY
CLKACCU
RISING EDGE MAY BE DELAYED BY READOUT
125 ns
125 ns
125 ns MIN
375ns
T0
T1
T2
T3
PHASE ERROR SIGN IS LATCHED AT T0 .
PHASE IS UPDATED AT T1 .
ACCU IS LOADED BETWEEN T2 AND T3 DEPENDING ON VME POSITION READOUT REQUEST.
ANTENNA ENCODERS
CLOCKS AND CONTROL LOGIC
Document Number
June 16, 1995
Sheet 6 of 8


LOCK-OUT DETECTOR
STATUS REGISTER
ANTENNA ENCODERS
STATUS
Title
Size Document Number REV
B
Date: November 28, 1994 Sheet 7 of 8
U15E
U15F
74HC14
U18
U17
GAL
LD
LU
/OVF
SPDONE
WATTREF
APDONE
UNLOCK
ERROR
STS[0..7]
/RST
UP
CLKPOS
CLKCMD
RDSTS
APD
SPW
SPD
LPFAIL
STGERR
REF
TEST


SHEET8
VME BACKPLANE
COMMANDS
INTERRUPTS
ADDRESS
DECODE
ANTENNA ENCODERS
VME INTERFACE
VECTOR BASE
UNUSED
BUSDIR=5V => WRITE
BUSDIR=0V => READ
GAL CODCMD
GAL CODITR
74AC645
74AC541
74S38
74ALS520
P65106
1N4148
CLKACCU
CLKCMD
SYSCLK
ACCESS
WRITE
SPREQ
APREQ
RDPOS
/AST
ITACK
CMDACK
/VDTACK
/VIRQ4
/VIACKIN
/VIACKOUT
IRQ
ERROR
APDONE
SPDONE
/VAM39
SYSCLK
VD[0..31]
VA[8..23]
ID[0..31]
STS[0..7]
STS[0..71]
A23/20
A19/16
A15/12
A11/8


VD[0..31]
VA[8..23]
AM = 39 OR 3D
(STANDARD ACCESS)
ANTENNA ENCODERS
VME BACKPLANE
Title
Size B
Document Number
REV
Date: December 6, 1994 Sheet 8 of 8
DIN41612 96/96
74HC154
+5V
+12V
-12V
VCC
VDD
VSS
/SYSCLK
/SYSRST
/VLWORD
/VDS1
/VDS0
/VWRITE
/VDTACK
/VAS
/VIACK
/VIACKIN
/VIACKOUT
/VIRQ7
/VIRQ6
/VIRQ5
/VIRQ4
/VIRQ3
/VIRQ2
/VIRQ1
/VAM39