

IRAM Plateau de Bure Observatory

DUAL LO2

User manual

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Revision E: commands 108, 109, 208 and 209 added for frequency offset implementation.

3. Introduction

The aim of the DUAL LO2¹ module is to deliver two LOs, at 8.1GHz and 9.9 GHz, to the IF band splitters. Each antenna output signal feeds a module that is located near the correlator.

The DUAL LO2 module is made of a digital-side board and 2 analog-side boards.

The digital-side board receives commands through the CAN³ bus, a micro-controller (MCU¹²) translates them and drives two Direct Digital Synthesizers¹¹ (DDS). Their action is synchronised by the 1SEC pulse issued from the observatory master clock.

Located on the analog-side board, two Phase Locked Loops (PLL¹²) are fed by the DDS 100MHz outputs. So, the 8.1GHz and 9.9GHz PLL outputs are controlled in phase and frequency.

Phase Locked Loop lock tuning voltages, power supply voltages, temperature and Identification informations can be monitored with few CAN¹² commands.

4. General Specifications

4.1 Background

The digital-side board carries two DDS, clock receivers, connectors and voltage regulators on the motherboard, and a C164⁶ micro-controller (MCU) located on a daughter board.

DDS¹² are AD9951YSV from Analog Devices with a 0.18 μ m technology and a core powered with 1.8V. Both are fed by a 100MHz reference clock that is multiplied by 4 with an on chip Phase Locked Loop (PLL) to drive the DDS core at 400MSPS. The DDS generates two 100MHz synchronous sine waves. The frequency and the phase of each output sine wave are synchronously set each second with new values. DDS output frequency resolution is 1 milliHertz and its phase resolution is 1 milliTurn (0.36 degree). DDS are controlled through a serial port compatible with the Serial Peripheral Interface (SPI¹²) standard.

The interface between the CAN bus and the SPI is a commercial daughter board with a C164 micro-controller (MCU). It is a derivative of the famous Infineon C167⁸ family. It receives commands through the CAN bus, computes data and translates them in SPI format. Interruption routines process CAN receive, timing management and SPI transmit. Frequency and phase updates are synchronised by the 1SEC timing signal. The MCU can be reset by an external RESET signal or by a local pushbutton located on the mother printed circuit board.

Each analog-side boards carries a PLL, clock receivers, connectors and voltage regulators. The 400MHz reference frequency of one PLL is multiplied by 20. Then the first 100MHz DDS output is added to generate the 8.1GHz frequency. The 400MHz reference frequency of the second PLL is multiplied by 25. Now the second

100MHz DDS output is subtracted to generate the 9.9GHz frequency. The DUAL LO2 outputs are 8.1GHz and 9.9GHz.

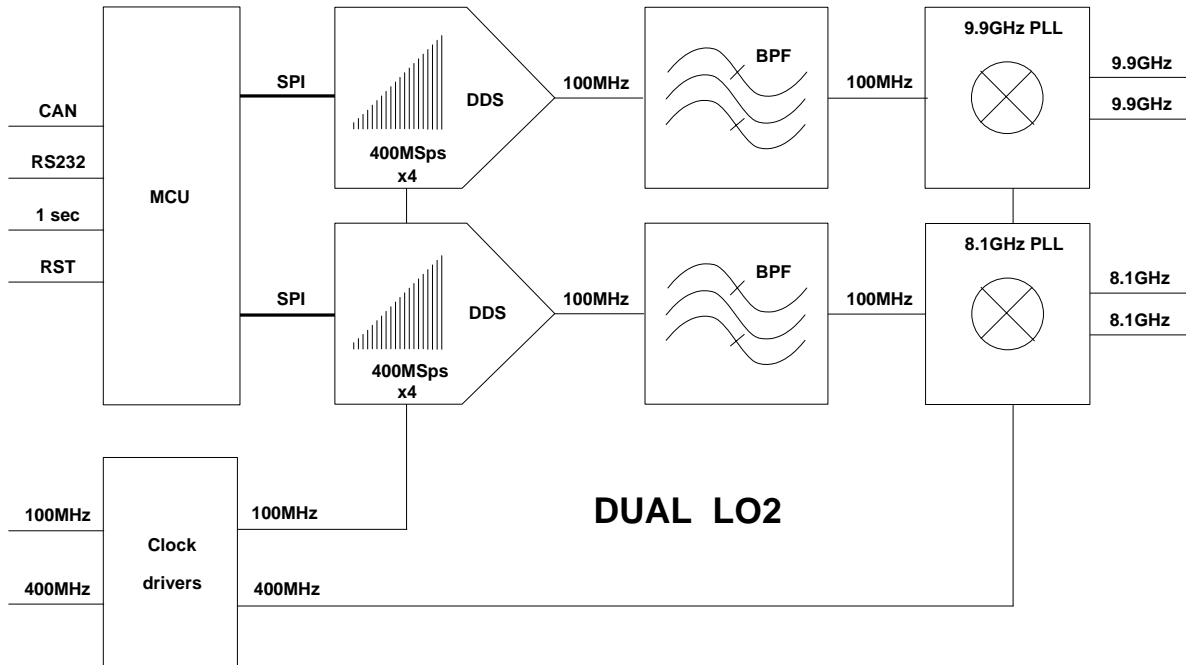


Figure 1: Block diagram

4.2 Power

The module requires a +6VDC/1.0A unregulated power supply, supplied through J3 connector on the module digital-side. The digital-side board draws 300mA and the analog-side boards draws 700mA.

The digital-side board also receives +12VDC through J4 connector, regulates to +10.5VDC and feeds the analog-side boards. The analog boards draw 25mA.

Total power requirement : +12V / 25mA + 6V / 1.0A

Note: no fuses are inside the module.

4.3 Operating Temperature Range

All components currently used have standard temperature range specifications of 0 – 70°C.

4.4 Printed circuit boards details

The digital-side board is a four-layer surface-mount printed circuit board and measures 110mm x 75mm.

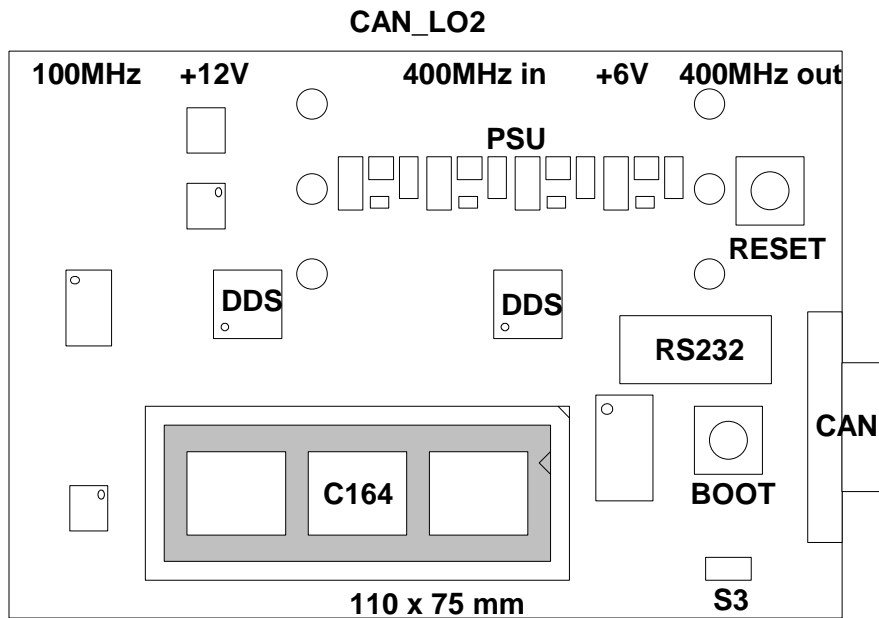


Figure 2: Digital-side PCB & components layout (real size)

The analog-side boards are four-layer surface-mount printed circuit boards and each measures 53mm x 75mm.

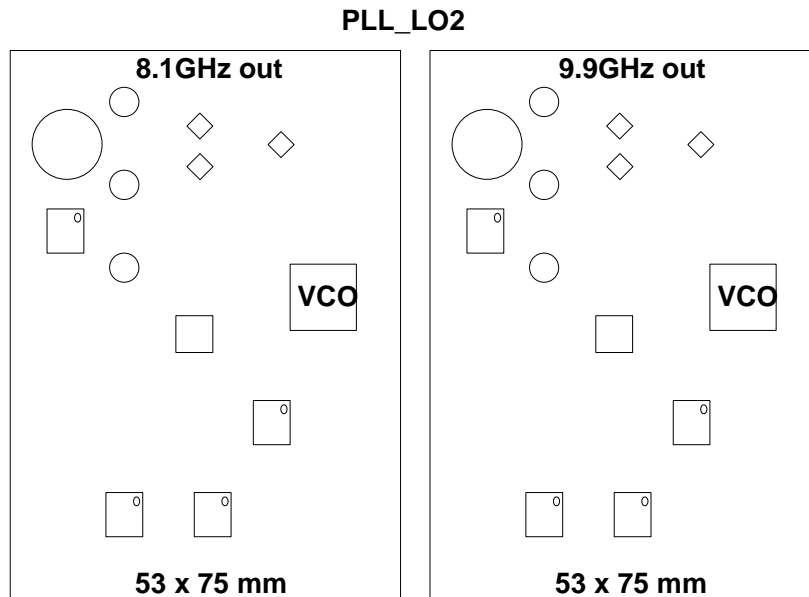


Figure 3: Analog-side PCBs & components layout (real size)

5. Device connections

5.1 Mechanical Details

The module is a metal box that measures 120mm x 32mm. Its height is 85mm.

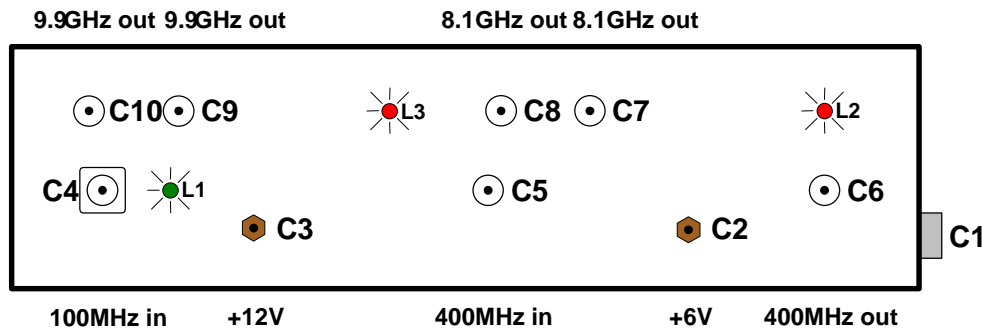


Figure 4: Module top view

5.2 Connectors

The module has several connectors located on the top of the module. Connectors are classified by function as it follows:

- C1: SubD-15 Connection to CAN bus including Reset and 1SEC timing signal inputs
- C2: +6V power supply input
- C3: +12V power supply input
- C4: 100MHz clock input (Subclck)
- C5: 400MHz clock input (SMA)
- C6: 400MHz reference output (SMA)
- C7: 8.1GHz PLL output H (SMA)
- C8: 8.1GHz PLL output V (SMA)
- C9: 9.9GHz PLL output H (SMA)
- C10: 9.9GHz PLL output V (SMA)
- J2: HE10 Connection to terminal RS232 (Access from inside only, on digital-side)

5.3 Indicators

The module has three external indicators located on the top of the module. Indicators are classified by function as it follows:

- L1: Module powered (flashes when a CAN frame is received or transmitted)
- L2: Lock alarm PLL 8.1GHz
- L3: Lock alarm PLL 9.9GHz

5.4 C1 connector pin-out

- C1: SUBD15 connection to CAN bus

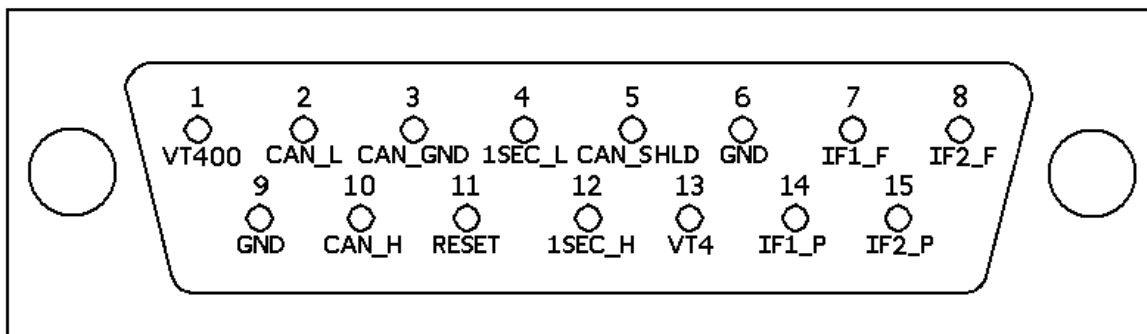


Figure 5: The DB15 male connector is shown view from the pin side

Pin	Signal	Dir	Function
1	Vt400	I	Tuning voltage of the 400MHz PLL
2	CAN_L	I/O	CAN_L Bus Line (dominant low)
3	CAN_GND	-	CAN ground, connected to board ground
4	1SEC_L	I	1 second Timing Signal, LVDS active low
5	CAN_SHLD	-	CAN shield, shorted to board ground
6	GND	-	Module ground
7	IF1_F	O	Select the IF1 Frequency (2 or 4 GHz)
8	IF2_F	O	Select the IF2 Frequency (2 or 4 GHz)
9	GND	-	Module ground
10	CAN_H	I/O	CAN_L Bus Line (recessive high)
11	Reset_L	I	Reset MCU line (low active)
12	1SEC_H	I	1 second Timing Signal, LVDS active high
13	VT4	I	Tuning voltage of the 4GHz PLL
14	IF1_P	O	Select the IF1 Polarization (Horizontal or Vertical)
15	IF2_P	O	Select the IF1 Polarization (Horizontal or Vertical)

Table 1: C1, CAN & Control connector pin outs

5.5 Internal connector pin-out (digital-side)

- J2: HE10 connection to terminal RS232 (Access from inside only)

Pin	Signal	Dir	Function
1	N/C	-	Not Connected
2	N/C	-	Not Connected
3	SERIAL_TxD	O	RS232 Transmit
4	N/C	-	Not Connected
5	SERIAL_RxD	I	RS232 Receive
6	N/C	-	Not Connected
7	N/C	-	Not Connected
8	N/C	-	Not Connected
9	GND	-	Board Ground
10	GND	-	Board Ground

Table 2: J2, RS232 connector pin outs

6. Instrument Interfaces

6.1 CAN bus I/O Signals

The DB15 socket C1 connects the module to the external CAN bus³ network. CAN_L & CAN_H feed a CAN transceiver (PCA82C251) located on the MCU daughter board. The CAN controller is embedded inside the MCU C164.

6.2 1SEC Sync interface

The 1SEC Timing signal is delivered in differential mode through the C1 connector described in paragraph 5.4 table 1. A DS90LV018A¹⁴ LVDS receiver, translates it to LVTTTL levels. The 1SEC timing signal feeds an fast interrupt input of the MCU to synchronize the events that takes place in the module.

6.3 Reset interface

The Reset signal is delivered in common mode through the C1 connector described in paragraph 5.4 table 1. Reset is active when the signal is grounded. The global Reset signal feeds the Master Reset of the C164 MCU. It is used to re-initialize the MCU.

6.4 RS232 Serial Port

The RS232 port is connected to a MAX233¹³, transceiver and levels translator, before feeding the asynchronous serial channel #0 of the MCU. This port is used to download the user software into the flash RAM. The HE10 socket J2, described in paragraph 5.5 table 2, is dedicated to maintenance and software upgrade. The 3M 10-pin connector J2 is only reachable when the module is open.

6.5 100MHz reference clock

The 100MHz reference clock input, AC coupled in single mode with 0dBm level, feeds a DS90LV019¹⁵ line receiver & driver. Its output feed the DDS using a differential line terminated by a 100 Ohms resistor.

6.6 Two 100MHz sine waves outputs

Both DDS generate a 100MHz sine wave controlled in frequency and phase. Between two 1SEC pulses, a CAN command requiring the next frequency and the next phase shift is processed by the MCU. Then the MCU delivers data through the SPI bus to the DDS. When the next 1SEC pulse occurs, the DDS immediately sets the new frequency and shifts the phase as required.

7. Local Interfaces

7.1 Synchronous Peripheral Interface (SPI)

A high speed Synchronous Serial Controller is embedded into the MCU to handle the SPI protocol. After initialisation, the interface is ready to handle 1Mbit/s serial rates. Four lines are used:

- SCLK for serial clock,
- MSIO for master transmit & slaves receive inputs and outputs,
- CS1 & CS2 for chips select.

We use the master transmit mode, thus the transmit clock (SCLK) is automatically generated while data is transmitted (MSIO). We don't receive any data. Transfers are performed MSB first.

A serial operation start with an instruction cycle, an 8-bit transfer which specify SEND or RECEIVE and the address of the register being accessed. Then a data byte transfer cycle follows. Data is loaded in the transmit register, CS is activated and serial transmit starts. As DDS have a 32-bit frequency register and a 14-bit phase register, so 5 consecutive bytes are required to set up the frequency or 3 consecutive bytes are required to set up the phase.

Now a new instruction cycle can take place specifying another register address we want to write into followed by another data byte transfer cycle.

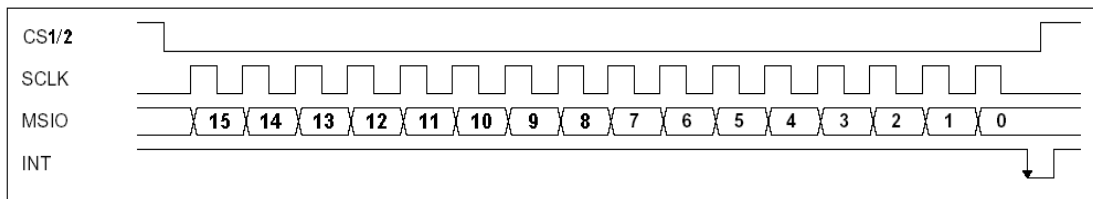


Figure 6: SPI data transfers

7.2 One Wire interface

Each motherboard has a unique serial ID number generated by a Dallas Semiconductor DS18S20¹² device, which offers a temperature sensor in addition. The serial ID number is delivered in 48-bit format (6 bytes) and temperature in 9 bits format (2 bytes). For maintenance purpose, module temperature and ID number can be requested with CAN commands.

7.3 Analog Voltages Monitoring

The MCU includes an on-chip 8-channel Analog to Digital Converter with 10-bit resolution. Four voltages available in the digital-side are monitored: +5V, +3.3V, +1.8V digital, +1.8V analog and four PLL tuning voltages: 400MHz, 4GHz, 8.1GHz and 9.9GHz. For maintenance purpose, voltages reading can be requested with few CAN commands.

ADC Channel	Signal	Dir	Function
0	+5V	I	Read +5.0V voltage
1	+3.3V	I	Read +3.3V voltage
2	+1.8V d	I	Read +1.8V digital voltage
3	+1.8V a	I	Read +1.8V analog voltage
4	Vt9_9	I	Read 9.9GHz PLL tuning voltage
5	Vt8_1	I	Read 8.1GHz PLL tuning voltage
6	Vt4	I	Read 4.0GHz PLL tuning voltage
7	Vt400	I	Read 400MHz PLL tuning voltage

Table 3: ADC channels assignment

8. Implementation Details

8.1 Micro Controller Unit (MCU)

The MCU is a DIPmodul-164⁴ from SYSTEC used as a daughter board. It carries an C164 microcontroller running at 20MHz with a 10MHz quartz, 128 KB of FLASH memory, 32 KB of SRAM, 2 KB of serial EEPROM, 8 dipswitches and a CAN transceiver. A single +5V / 80mA power supply is required. According to SYSTEC, its MTBF is 1,307,950 hours or 149 years.

8.1.1 C164 Micro-Controller Unit (MCU)

The micro-controller is a C164⁶, a 16-bit processor from INFINEON. It is a derivative of the C167⁸ family in an 80-pin TQFP package. It combines high CPU performance (up to 10 MIPS) with high peripheral functionality: full CAN interface, 8-input ADC, asynchronous serial port, High Speed synchronous serial port, timers, RTC¹², 14 digital I/Os available to user and high speed DMA under interruption. A bootstrap loader is available to download user software into Flash memory. For more information, refer to the datasheet listed at the end the document⁴.

8.1.2 CAN Controller

The micro-controller has an on-chip CAN controller (Rev. 2.0B) with 15 message objects. It is capable of 1-Mbaud operations.

8.1.3 Analog to Digital Converter

The micro-controller has an 8-channel Analog to Digital Converter with 10-bit resolution. A conversion can take place in less than 10 microseconds. Any unused channel can be used as an extra conventional digital input.

8.1.4 Digital I/O

The micro-controller has up to 59 general purpose I/Os among which 14 are available outside of the daughter board. This is enough for our application.

8.1.5 Asynchronous Serial Controller

The micro-controller has a single serial channel dedicated to the RS232 interface. This interface is used to download user software.

8.1.6 Synchronous Serial Controller

The micro-controller has a high-speed synchronous serial channel capable of 5-Mbaud operations. It can be used for: I2C, SPI or any serial transmission. In this module, it is dedicated to communicate with an EEPROM and is not available on external pins.

8.1.7 One Wire controller

One-Wire interfacing has easily been developed in C for this micro-controller. This interface use one pin and is dedicated to DALLAS integrated circuits.

8.2 Direct Digital Synthesizers (DDS)

Direct Digital Synthesizers are the ultra low power AD9951¹¹ capable of 400MSPS¹². It is made of 0.18 μ m CMOS technology powered by only 1.8V / 200mW. Fed by a 100MHz clock, the on chip PLL generates a 400MHz used as master clock, a 32-bit frequency tuning register and a 14-bit phase register are added into a phase accumulator to produce a phase ramp. The phase ramp is converted to a digital sine wave through a ROM table and feeds a 14-bit Digital to Analog Converter. The DDS output is a 400MHz pseudo analog sine wave. A SPI serial bus feeds its registers. For more information, refer to the datasheet listed at the end the document.

8.3 Voltage regulators

Four ultra low drop voltage regulators in SOT23-5 package are used in this module. Fed by +6V, the four regulators deliver:

- +5.0V / 80mA for the MCU
- +3.3V / 40mA for the DDS Digital I/O + interfaces
- +1.8V / 50mA for the DDS Digital core
- +1.8V / 130mA for the DDS Analog core

8.4 8.1GHZ and 9.9GHZ PLL (analog-side boards)

The two 100MHz sine waves delivered by the DDS feed a 100MHz band pass filter and extend to each PLL located on the opposite side of the module. A 400MHz power splitter feeds the two PLL RF inputs. The first PLL generates an 8.1GHz frequency and the second PLL generates a 9.9GHz frequency.

The 2 analog-side boards are powered by +6V / 700mA and +12V / 25mA.

9. Built-in Firmware

9.1 Bootstrap loader

A bootstrap loader is available to download user software. By simultaneously pressing RESET and BOOT then release first RESET, and 3 seconds later release BOOT. Now the MCU is ready to accept user software from the RS232 line. Run Flashtools16W on any PC to download the firmware into the FLASH memory. At the end of the download process, pressing RESET will initialise the program.

9.2 Power up or Reset sequence

When the rack is either powered up or reset, a green LEDs L1 goes on upon successful completion of the initialisation test. PLLs are intialized with no phase shift and the module is ready to receive CAN frames. After a warming up time, both red LEDs should stay off. At init, each IFextender selects 4 GHz LO with horizontal polarisation to feed the narrow band correlator. IF1 → 4200-5200 MHz & IF2 → 6000-7000 MHz.

10. Device-Specific Software / CAN Functions Interface

10.1 Operating program

In normal operation, the module receives Can frames with next frequency and phase settings. The 1sec pulse synchronizes all PLL changes.

10.2 CAN Overview

The Dual LO2 module is controlled and monitored by the PdB² CAN network, revision 2.0B (extended format), operating at 1Mbauds. The module is a slave CAN node operating in the address range 0x0800 0000 (hex), through 0x081F 0000 (hex).

Its CAN relative address space spans from 0x0 0000 to 0x3 FFFF (hex). 8 switches located on the MCU daughter board define the module global address. Each switch being a power of 2, the result ranging from 0 up to 255 is multiplied by 0x4 0000 (hex) to generate the module global address. When a broadcast message 0 is received, the module transmits its address. CAN payload bytes are listed from 1 up to 8.

Address range	0x0800 0000	0x08FF FFFF (hex)
Relative address	0x0000 0000	0x0003 FFFF (hex)
Example:		
Module 1 global address	0x0800 0000	0x0803 FFFF (hex)
Module 2 global address	0x0804 0000	0x0807 FFFF (hex)
Module 3 global address	0x0808 0000	0x080B FFFF (hex)
Module 4 global address	0x080C 0000	0x080F FFFF (hex)
Module 5 global address	0x0810 0000	0x0813 FFFF (hex)
Module 6 global address	0x0814 0000	0x0817 FFFF (hex)

Note: L1 indicator flashes when a CAN frame is received or transmitted.

10.3 Summary of the CAN Monitor points

<i>Name</i>	<i>Relative CAN Address (hex)</i>	<i>Data Size (Bytes)</i>	<i>Target</i>	<i>Timing Event Related?</i>
MODULE_ID	0x0 00 00	8	Maintenance	No
SERIAL_&_TEMP	0x0 00 01	8	Maintenance	No
PSU_VOLTAGE	0x0 00 02	8	Maintenance	No
PLL_TUNING_VOLTAGE	0x0 00 03	8	Operation	No
MODULE_STATUS	0x0 00 04	6	Maintenance	No
LAST_F_OFFSET&_PHASE	0x0 02 00	8	Maintenance	No
LAST_FREQUENCY_LOW	0x0 02 01	7	Maintenance	No
LAST_FREQUENCY_UP	0x0 02 02	7	Maintenance	No
LAST_PHASE_LOW	0x0 02 03	3	Maintenance	No
LAST_PHASE_UP	0x0 02 04	3	Maintenance	No
LAST_SELECT_IF	0x0 02 05	4	Maintenance	No
LAST_8G1_OFFSET&_PHASE	0x0 02 08	6	Maintenance	No
LAST_9G9_OFFSET&_PHASE	0x0 02 09	6	Maintenance	No

Table 4: Summary of Monitor Points

10.4 Summary of the CAN Control points

<i>Name</i>	<i>Relative CAN Address (hex)</i>	<i>Data Size (Bytes)</i>	<i>Target</i>	<i>Timing Event Related?</i>
FREQ_OFFSET_&_PHASE	0x0 01 00	8	Operation	Yes
FREQUENCY	0x0 01 01	7	Maintenance	No
PHASE	0x0 01 02	3	Maintenance	No
SELECT_IF	0x0 01 03	4	Operation	No
8G1_OFFSET_&_PHASE	0x0 01 08	6	Operation	Yes
9G9_OFFSET_&_PHASE	0x0 01 09	6	Operation	Yes
INIT_DDS	0x0 01 F0	1	Operation	No
CPU_RESET	0x0 01 FF	1	Operation	No

Table 5: Summary of Control Points

10.5 CAN payload contents

10.5.1 Monitor points in detail

a) MODULE_ID

Relative CAN Address	0x0 00 00
Description	This monitor point returns the module ID and waste.
Target	Maintenance
TE Related	No
Data	8 bytes: Byte 1: Integrated circuit family code Byte 2, 3, 4, 5, 6 & 7: 48 bits serial number Byte 8: CRC

b) SERIAL_&_TEMP

Relative CAN Address	0x0 00 01
Description	This command returns the module serial number followed by its internal temperature. The answer is sent within 2 seconds.
Target	Maintenance (<i>never use it during operation!</i>)
TE Related	No
Data	8 bytes: Byte 1, 2, 3, 4, 5 & 6: 48 bits serial number Byte 7 & 8: Module temperature
Conversion factor	Temperature = First Byte + Second Byte/100
Operating Range	15°C - 55°C recommended range

c) PSU_VOLTAGE

Relative CAN Address	0x0 00 02
Description	<i>This monitor point indicates the measured voltages of the Power Supplies.</i>
Target	<i>Maintenance</i>
TE Related	<i>No</i>
Data	8 bytes: <i>Byte 1 & 2: 1.8V Analog (0.00-5.00)</i> <i>Byte 3 & 4: 1.8V Digital (0.00-5.00)</i> <i>Byte 5 & 6: 3.3V Digital (0.00-5.00)</i> <i>Byte 7 & 8: 5.0V Digital (0.00-5.00)</i>
Conversion factor	<i>Voltage = First Byte + Second Byte/100</i>
Operating Range	<i>1.8V Analog -> (1.70-1.90)</i> <i>1.8V Digital -> (1.70-1.90)</i> <i>3.3V Digital -> (3.15-3.45)</i> <i>5.0V Digital -> (4.75-5.25)</i>

d) PLL_TUNING_VOLTAGE

Relative CAN Address	0x0 00 03
Description	<i>This command returns the measured voltages of the Lock Indicators.</i>
Target	<i>Operation</i>
TE Related	<i>No</i>
Data	8 bytes: <i>Byte 1 & 2: 400MHz PLL tuning voltage (0.00-5.00)</i> <i>Byte 3 & 4: 4.0GHz PLL tuning voltage (0.00-5.00)</i> <i>Byte 5 & 6: 8.1GHz PLL tuning voltage (0.00-5.00)</i> <i>Byte 7 & 8: 9.9GHz PLL tuning voltage (0.00-5.00)</i>
Conversion factor	<i>Voltage = First Byte + Second Byte/100</i>
Operating Range	<i>1.5 – 5.0 Volts</i>

e) MODULE_STATUS

Relative CAN Address	0x0 00 04
Description	<i>This monitor point reports the CAN bus reliability, the firmware revision date and the Timer7 value.</i>
Target	<i>Maintenance</i>
TE Related	<i>No</i>
Data	6 bytes: <i>Byte 1: CAN bus errors (0-255)</i> <i>Byte 2, 3, 4: Firmware revision date Day, Month, Year</i> <i>Byte 5 & 6: Timer7 content (15 536 +/-10)</i>

f) **LAST_F_OFFSET&_PHASE**

Relative CAN Address	0x0 02 00
Description	This monitor point reports the last offset frequency and initial phase command sent to the Dual LO2 module.
Target	Maintenance
TE Related	No
Data	8 bytes: Byte 1 & 2: LO2U Offset frequency in milliHertz (+/-32 000) Byte 3 & 4: LO2U Initial phase in milliTurn (0-999) Byte 5 & 6: LO2L Offset frequency in milliHertz (+/-32 000) Byte 7 & 8: LO2L Initial phase in milliTurn (0-999) Note: If no data was received since last reset the answer will hold the default set-up.
Conversion factor	Data = 256 x First Byte + Second Byte

g) **LAST_FREQUENCY_LOW**

Relative CAN Address	0x0 02 01
Description	This monitor point reports the last frequency command sent to the Dual LO2 module.
Target	Maintenance
TE Related	No
Data	7 bytes: Byte 1: LO2 target = 1 Byte 2, 3, 4 & 5: Main frequency in Hertz (0-160 000 000) Byte 6 & 7: Offset frequency in milliHertz (+/-32 000)
Conversion factor	Main frequency = 167777216 x First Byte + 65536 x Second Byte + 256 x Third Byte + Fourth Byte Offset frequency = 256 x First Byte + Second Byte Note: If no data was received since last reset the answer will hold the default set-up.

h) **LAST_FREQUENCY_UP**

Relative CAN Address	0x0 02 02
Description	This monitor point reports the last frequency command sent to the Dual LO2 module.
Target	Maintenance
TE Related	No
Data	7 bytes: Byte 1: LO2 target = 0 Byte 2, 3, 4 & 5: Main frequency in Hertz (0-160 000 000) Byte 6 & 7: Offset frequency in milliHertz (+/-32 000)
Conversion factor	Main frequency = 167777216 x First Byte + 65536 x Second Byte + 256 x Third Byte + Fourth Byte Offset frequency = 256 x First Byte + Second Byte Note: If no data was received since last reset the answer will hold the default set-up.

i) **LAST_PHASE_LOW**

Relative CAN Address	0x0 02 03
Description	<i>This monitor point reports the last phase command sent to the Dual LO2 module.</i>
Target	<i>Maintenance</i>
TE Related	<i>No</i>
Data	3 bytes: <i>Byte 1: LO2 target = 1</i> <i>Byte 2 & 3: Initial phase in milliTurn (0-999)</i> <i>Note: If no data was received since last reset the answer will hold the default set-up.</i>
Conversion factor	<i>Data = 256 x First Byte + Second Byte</i>

j) **LAST_PHASE_UP**

Relative CAN Address	0x0 02 04
Description	<i>This monitor point reports the last phase command sent to the Dual LO2 module.</i>
Target	<i>Maintenance</i>
TE Related	<i>No</i>
Data	3 bytes: <i>Byte 1: LO2 target = 0</i> <i>Byte 2 & 3: Initial phase in milliTurn (0-999)</i> <i>Note: If no data was received since last reset the answer will hold the default set-up.</i>
Conversion factor	<i>Data = 256 x First Byte + Second Byte</i>

k) **LAST_SELECT_IF**

Relative CAN Address	0x0 02 05
Description	<i>This monitor point reports the last IF bands select command sent to the Dual LO2 module.</i>
Target	<i>Maintenance</i>
TE Related	<i>No</i>
Data	4 bytes: <i>Byte 1: Select IF1_Freq (0-1) : 0 = 2GHz / 1 = 4GHz</i> <i>Byte 2: Select IF2_Freq (0-1) : 0 = 2GHz / 1 = 4GHz</i> <i>Byte 3: Select IF1_Pol (0-1) : 0 = Vertical / 1 = Horizontal</i> <i>Byte 4: Select IF2_Pol (0-1) : 0 = Vertical / 1 = Horizontal</i> <i>Note: If no data was received since last reset the answer will hold the default set-up.</i>

l) LAST_8G1_OFFSET&_PHASE

Relative CAN Address	0x0 02 08
Description	<i>This monitor point reports the last 8.1 GHz offset frequency and initial phase command sent to the Dual LO2 module.</i>
Target	<i>Maintenance</i>
TE Related	<i>No</i>
Data	<p>6 bytes:</p> <p>Byte 1 & 2 & 3 & 4: 8.1 GHz frequency offset in milliHertz (+/- 2 000 000 000)</p> <p>Byte 5 & 6: 8.1 GHz initial phase in milliTurn (0-999)</p> <p>Note: If no data was received since last reset the answer will hold the default set-up.</p>
Conversion factor	<p>$Data = 2^{24} \times \text{First Byte} + 2^{16} \times \text{Second Byte} + 2^8 \times \text{Third Byte} + \text{Fourth Byte}$</p> <p>$Data = 256 \times \text{Fifth Byte} + \text{Sixth Byte}$</p>

m) LAST_9G9_OFFSET&_PHASE

Relative CAN Address	0x0 02 09
Description	<i>This monitor point reports the last 9.9 GHz offset frequency and initial phase command sent to the Dual LO2 module.</i>
Target	<i>Maintenance</i>
TE Related	<i>No</i>
Data	<p>6 bytes:</p> <p>Byte 1 & 2 & 3 & 4: 9.9 GHz frequency offset in milliHertz (+/- 2 000 000 000)</p> <p>Byte 5 & 6: 9.9 GHz initial phase in milliTurn (0-999)</p> <p>Note: If no data was received since last reset the answer will hold the default set-up.</p>
Conversion factor	<p>$Data = 2^{24} \times \text{First Byte} + 2^{16} \times \text{Second Byte} + 2^8 \times \text{Third Byte} + \text{Fourth Byte}$</p> <p>$Data = 256 \times \text{Fifth Byte} + \text{Sixth Byte}$</p>

10.5.2 Control points in detail

a) **FREQ_OFFSET_&_PHASE**

Relative CAN Address	0x0 01 00
Description	This command specifies the Dual LO2 frequency offsets and initial phases over the next second interval. It is the most frequent command that will be sent to this device every second.
Target	Operation
TE Related	<i>Yes. The command should reach the Dual LO2 module a least 50 milliseconds before the next second to be serviced on time.</i>
Data	8 bytes: Byte 1 & 2: LO2U Offset frequency in milliHertz (+/-32 000) Byte 3 & 4: LO2U Initial phase in milliTurn (0-999) Byte 5 & 6: LO2L Offset frequency in milliHertz (+/-32 000) Byte 7 & 8: LO2L Initial phase in milliTurn (0-999)
Conversion factor	$Data = 256 \times \text{First Byte} + \text{Second Byte}$

b) **FREQUENCY**

Relative CAN Address	0x0 01 01
Description	This command specifies a new frequency for the LO2. The action is immediate.
Target	Maintenance
TE Related	No
Data	7 bytes: Byte 1: LO2 target (0= U; 1=L) Byte 2, 3, 4 & 5: Main frequency in Hertz (0-160 000 000) Byte 6 & 7: Offset frequency in milliHertz (+/-32 000)
Conversion factor	$\text{Main frequency} = 167777216 \times \text{First Byte} + 65536 \times \text{Second Byte} + 256 \times \text{Third Byte} + \text{Fourth Byte}$ $\text{Offset frequency} = 256 \times \text{First Byte} + \text{Second Byte}$

c) **PHASE**

Relative CAN Address	0x0 01 02
Description	This command specifies a new phase for the LO2. The action is immediate.
Target	Maintenance
TE Related	No
Data	3 bytes: Byte 1: LO2 target (0= U ; 1=L) Byte 2 & 3: Initial phase in milliTurn (0-999)
Conversion factor	$Data = 256 \times \text{First Byte} + \text{Second Byte}$

d) SELECT_IF

Relative CAN Address	<i>0x0 01 03</i>
Description	<i>This command select the IF bands to be processed by the narrow band correlator. Selections are made through the IF extender module. It should be the first command sent to this device before every sky observations.</i>
Target	<i>Operation</i>
TE Related	<i>No</i>
Data	<i>4 bytes: Byte 1: Select IF1_Freq LO (0-1) : 0 = 2GHz / 1 = 4GHz Byte 2: Select IF2_Freq LO (0-1) : 0 = 2GHz / 1 = 4GHz Byte 3: Select IF1_Pol (0-1) : 0 = Vertical / 1 = Horizontal Byte 4: Select IF2_Pol (0-1) : 0 = Vertical / 1 = Horizontal Note: when initialised, selected LOs are 4GHz & Horizontal inputs. IF1 → 4200-5200 MHz & IF2 → 6000-7000 MHz.</i>

e) INIT_DDS

Relative CAN Address	<i>0x0 01 F0</i>
Description	<i>This command initialises both DDS with their default values.</i>
Target	<i>Operation</i>
TE Related	<i>No</i>
Data	<i>1 byte: Byte 1: Don't care</i>

f) CPU_RESET

Relative CAN Address	<i>0x0 01 FF</i>
Description	<i>This command initialises the Dual LO2 MCU.</i>
Target	<i>Operation</i>
TE Related	<i>No</i>
Data	<i>1 byte: Byte 1: Don't care</i>

g) 8G1_OFFSET_&_PHASE

Relative CAN Address	0x0 01 08
Description	This command specifies the 8.1 GHz frequency offset and its initial phase over the next second interval. It is the most frequent command that will be sent to this device every second.
Target	Operation
TE Related	<i>Yes. The command should reach the Dual LO2 module a least 50 milliseconds before the next second to be serviced on time.</i>
Data	6 bytes: Byte 1 & 2 & 3 & 4: 8.1 GHz frequency offset in milliHertz (+/- 2 000 000 000) Byte 5 & 6: 8.1 GHz initial phase in milliTurn (0-999)
Conversion factor	$Data = 2^{24} \times \text{First Byte} + 2^{16} \times \text{Second Byte} + 2^8 \times \text{Third Byte} + \text{Fourth Byte}$ $Data = 256 \times \text{Fifth Byte} + \text{Sixth Byte}$

h) 9G9_OFFSET_&_PHASE

Relative CAN Address	0x0 01 09
Description	This command specifies the 9.9 GHz frequency offset and its initial phase over the next second interval. It is the most frequent command that will be sent to this device every second.
Target	Operation
TE Related	<i>Yes. The command should reach the Dual LO2 module a least 50 milliseconds before the next second to be serviced on time.</i>
Data	6 bytes: Byte 1 & 2 & 3 & 4: 9.9 GHz frequency offset in milliHertz (+/- 2 000 000 000) Byte 5 & 6: 9.9 GHz initial phase in milliTurn (0-999)
Conversion factor	$Data = 2^{24} \times \text{First Byte} + 2^{16} \times \text{Second Byte} + 2^8 \times \text{Third Byte} + \text{Fourth Byte}$ $Data = 256 \times \text{Fifth Byte} + \text{Sixth Byte}$

11. Test Software

The Dual LO2 module can be controlled and monitored by the “Dual_LO2_test.vi”. It can be run with LABVIEW from any PC hosting a CAN interface. The test equipment is self-teaching and a view of the its control screen is displayed next:

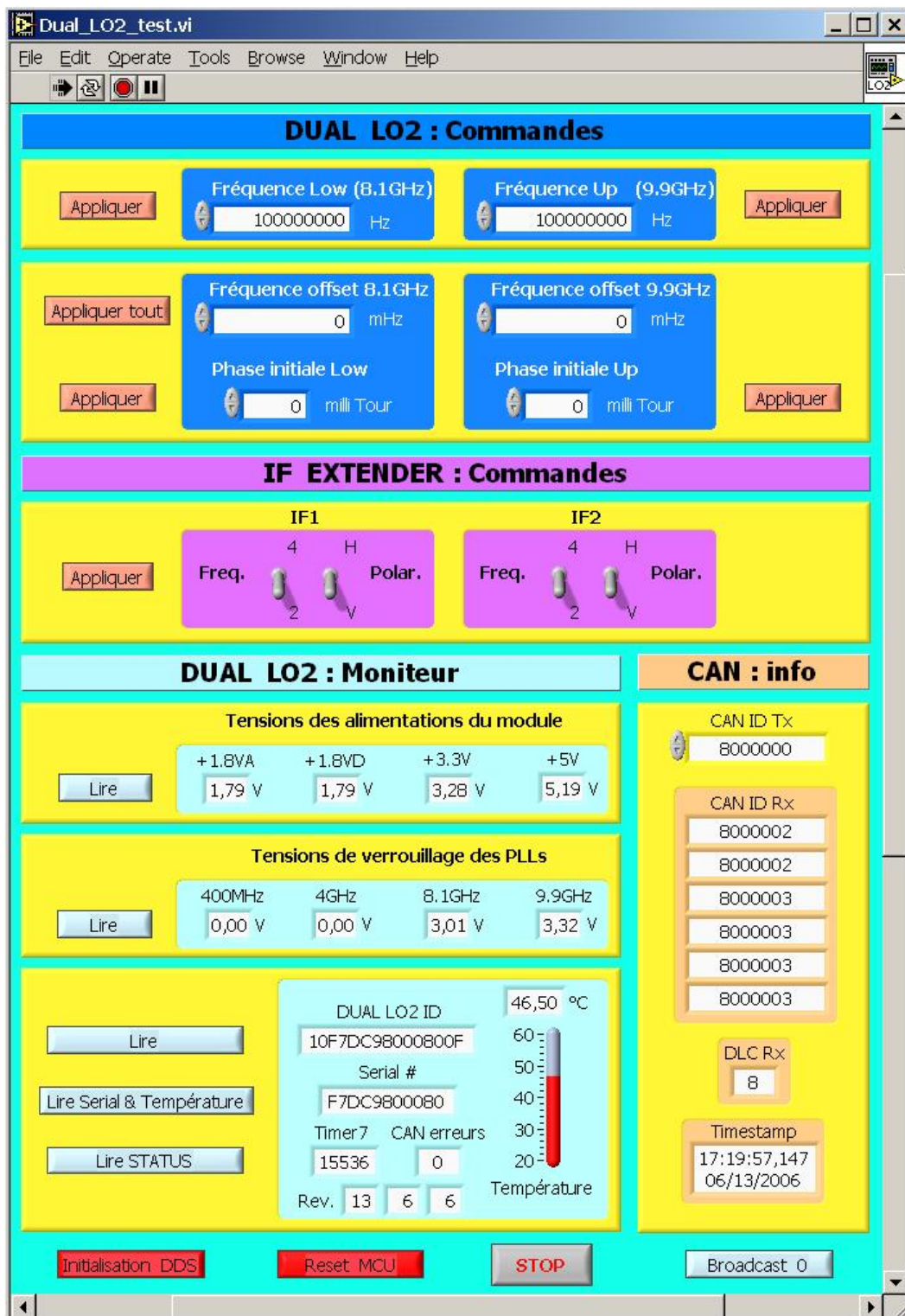


Figure 7: Dual LO2 test panel

12. Abbreviations and Acronyms

1SEC	PdB reference timing with TTL signalling
ADC	Analog to Digital Converter
C164	Reduced version of the C167 (Infineon – Siemens)
C167	16-bit micro-controller of the C166 family (Infineon – Siemens)
CAN	Controller Area Network, field bus dedicated to control. (Bosch)
CPU	Central Processing Unit
DDS	Direct Digital Synthesizer
DMA	Direct Memory Access
EEPROM	Electrically Erasable & Programmable Read Only Memory
FLASH	Permanent memory that can be reprogrammed
I/O	Inputs and Outputs
LSB / MSB	Least Significant Bit / Most Significant Bit
MSPS	Mega Samples per Second
MCU	Micro Controller Unit
MTBF	Mean Time Between Failures
One-Wire	Serial bus using one wire with ground return (DALLAS)
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Locked Loop, generates a sine wave multiple of the reference clock
RS232	Standard computer interface for serial communication with a terminal
RTC	Real Time Clock
SPI	Synchronous Peripheral Interface (Motorola)
VCO	Voltage Controlled Oscillator

13. References

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16. LP2985, Micropower 150mA low noise ultra low dropout regulator, data sheet, January 2003, National Semiconductor.
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14. Dual LO2 Drawing List

CANLO8_10 interface

DDS1 @ 100MHz

DDS2 @ 100MHz

Power supplies

400MHz Coupler and +10.5V voltage regulator

8GHz PLL

10GHz PLL