IRAM-COMP-020

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22GHz VME Board

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Keywords:

Approved by:	Date:	Signature:
A.Perrigouard	December 2005	

Change Record

REVISION	DATE	AUTHOR	SECTION/PAGE AFFECTED	REMARKS
1	July 8 2004	Francis Morel		

Contents

1 22G VME Board description:

This board was specifically designed to control the 22G Receiver.
The board connects to the Receiver through 12 low-cost plastic fiber optics, to avoid interferences and ground loops.
It connects to the Interferometer “TU01” (1 Hz) pulse, fed to all antennas from the GPS time base, through a front-panel BNC connector. This input signal is used to (re)synchronize a local oscillator.
The board generates an interrupt and latches the status and the data from the Receiver upon each valid "TU01" pulse. The vector used by the interrupt depends on the board status: If the board is unlocked (not synchronized with TU01), the vector ERROR will be used. Otherwise, vector OK.
The main parts of this board are 6 [31-bit + overflow] counters, used to integrate the V-to-F outputs of the Receiver. These counters are first registered and then cleared upon each "TU01" pulse. The blanking (lost each second) time is typically 180 nanoseconds.
The board was built using a FPGA Altera EPF10K30.
The VME BUS is used as a 16-bit wide bus (D16 norm). This implies that each readout of a 32-bit word needs 2 accesses on the VME Bus.

1.1 Fiber outputs TO the receiver :

CMD_ LOAD_ON	Lit fiber moves the reference load in front of the receiver.	Static command bit
CMD_NOISE_ON	Lit fiber turns ON the noise diode of the receiver.	Static command bit
CMD_PWR	Unused, but functional	Static command bit

1.2 Fiber inputs FROM the Receiver:

LOAD_ON	Fiber is lit if the Reference Load is in front of the Receiver	Static Status bit
2 MHz Reference	V/F reference frequency	Frequency encoded signal
LOAD_T	Reference Load temperature	Frequency encoded signal
PELTIER_T	Peltier regulator temperature	Frequency encoded signal
ALARM	Receiver alarm	Static Status bit
F3	Channel 3	Frequency encoded signal
F2	Channel 2	Frequency encoded signal
F1	Channel 1	Frequency encoded signal
F0	Channel 0	Frequency encoded signal

1.3 22G registers addresses:

. All the registers are mapped in the A16/D16 VME I/O space => Address Modifier=29/2D.The board uses 128 word (even) addresses (XX00 to XXFE). The board Base-address bits [15-8] are selectable using 2 encoding wheels, **RC1 [A15-A12]**, and **RC2 [A11-A08].**
The actual VME address on Plateau de Bure of the 22G Board is 0xFFFF1000

1.4 Input registers (read-only):

Channel 0 LSW	Base-address + 0x0	Channel 0 [15..0]
Channel 0 MSW	Base-address + 0x2	Bit 15 = Overflow Bits [14..0]=Channel 0 [30..16]
Channel 1 LSW	Base-address + 0x4	Channel 1 [15…0]

Channel 1 MSW	Base-address + 0x6	Bit 15 = Overflow Bits [14..0]=Channel 1 [30..16]
Channel 2 LSW	Base-address + 0x8	Channel 2 [15…0]
Channel 2 MSW	Base-address + 0xA	Bit 15 = Overflow Bits [14..0]=Channel 2 [30..16]
PELTIER_T LSW	Base-address + 0xC	Peltier temp[15...0]
PELTIER_T MSW	Base-address + 0xE	Bit 15 = Overflow Bits [14..0]=Load temp [30..16]
LOAD_T LSW	Base-address + 0x10	Peltier temp [15...0]
LOAD_T MSW	Base-address + 0x12	Bit 15 = Overflow Bits [14..0]=Load temp [30..16]
2 MHZ LSW	Base-address + 0x14	2 MHz Ref [15..0]
2 MHZ MSW	Base-address + 0x16	Bit 15 = Overflow Bits [14..0]=2MHz Ref [30..16]
Channel 3 LSW	Base-address + 0x18	Channel 3 [15…0]
Channel 3 MSW	Base-address + 0x1A	Bit 15 = Overflow Bits [14..0]=Channel 3 [30..16]

1.5 Vectors register (read-only):

Vector OK LSByte	Base-address + 0x1C	Bits [3..0] = Vector OK [3..0]
Vector ERROR LSByte	Base-address + 0x1C	Bits [11..8]=Vector ERROR [3..0]

1.6 Status register (read-only): Base-address + 0x1E

N.B : Status register bits are latched upon “TU01” interrupt edge.

15	14..6	5	4	3	2	1	0
ERR	XX	ALARM	UNL	IT_ENA	NOISE_ON	LOAD_ON	XX

Description of the STS register bits :

Bit 15	ERR	ERR = ALARM + UNL
Bits [14..6]	XX	Don’t care
Bit 5	ALARM	Set if Receiver Alarm is ON
Bit 4	UNL	Set when the board is not synchronized with “TU01”
Bit 3	IT_ENA	Set when the interrupt has been enabled (see Command Register)
Bit 2	NOISE_ON	Set when the Noise Diode has been requested to turn ON. This bit is **NOT** read from the receiver
Bit 1	LOAD_ON	Set when the Reference Load is in front of the Receiver
Bit 0	XX	Don’t care

1.7 Vectors registers (write-only):

Vector OK	Base-address + 0x1A	Bits [3..0] = Vector OK [3..0] Vector OK [7..4] are switch-selectable (S1)
Vector ERROR	Base-address + 0x1C	Bits [3..0] = Vector ERROR [3..0] Vector ERROR [7..4] are switch-selectable (S1)

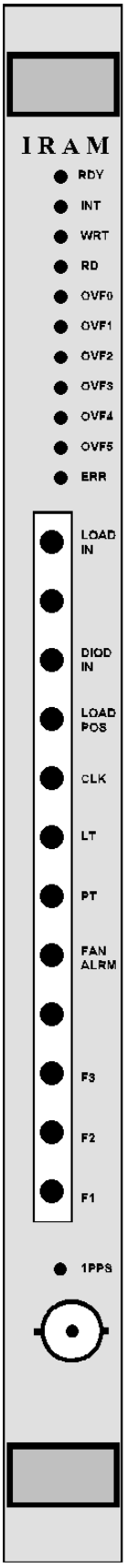
1.8 Command Register (write-only): Base-address + 0x1E

15..4	3	2	1	0
XX	CMD_IT_ENA	CMD_NOISE_ON	CMD_LOAD_ON	CMD_PWR

Description of the CMR bits :

Bits [15..4]	XX	Don't care
Bit 3	CMD_IT_ENA	When set, enables interrupt generation. Cannot be set if both vectors (OK and ERROR) have not been defined first.
Bit 2	CMD_NOISE_ON	When set, turns On the Noise Diode.
Bit 1	CMD_LOAD_ON	When set, moves the Load in front of the Receiver.
Bit 0	CMD_PWR	Unused, but functional

1.9 22G Board Front-Panel:



Red LEDs are used for displaying ERROR conditions only.

From top to bottom:

11 LEDs :

READY	Green	The interrupt is enabled AND the board is synchronized
INT	Yellow	ON when an interrupt request is active
WRT	Yellow	Will flash upon each “write” access
READ	Yellow	Will flash upon each “read” access
OVF0	Red	Channel 0 Overflow
OVF1	Red	Channel 1 Overflow
OVF2	Red	Channel 2 Overflow
OVF3	Red	Channel 3 Overflow
OVF4	Red	Peltier_T Overflow
OVF5	Red	Load_T Overflow
ERR	Red	The Altera chip did not initialize upon power-on

N.B: All leds "OVFx" will blink if ALARM = 1.

3 optical outputs (see Command register)

Output name	**Signal name**	**Comments**
LOAD IN	CMD_LOAD_ON	When ON, move the reference load in front of the receiver
	CMD_PWR	Unused in actual design, but functional
DIOD IN	CMD_NOISE_ON	When ON, turns ON the noise diode of the receiver

9 optical inputs (see Status register)

Input name	**Signal name**	**Comments**
LOAD POS	LOAD_ON	Turns ON when the reference load is in front of the receiver
CLK	2 MHZ	2 MHz reference from the receiver
LT	LOAD_T	Reference Load temperature measurement
PT	PELTIER_T	Peltier cooler temperature measurement
FAN ALRM	ALARM	Receiver alarm
	F3	Channel 3 measurement
F3	F2	Channel 2 measurement
F2	F1	Channel 1 measurement
F1	F0	Channel 0 measurement

1 yellow LED:
"pps" pulse, "TU01" resynchronized and regenerated by the board.

1 BNC connector:
"TU01" input.

1.10 Synchronization:

Upon start-up, the board is in "start" mode and generates no interrupt.
It accepts the first "TU01" pulse it receives, starts its internal base-time, and waits for the next pulse. If this next pulse is received within 1 second +/- 4 milliseconds, the board goes into "synchronized" mode, accepting only the pulses separated by 1+/- 4e-3 seconds, resynchronizing on each of these pulses, and generating each time an interrupt (if the bit CMD_IT_ENA has been set in the Command register).
Glitches are thus eliminated.
If the "TU01" pulse is missing, the board will then internally supply this pulse and still generate the interrupt, but no more than 32 times. After a delay of 32 seconds without having received any "TU01" pulse, the board will go back into "start" mode and stop generating interrupts and latching data.

1.11 Getting started:

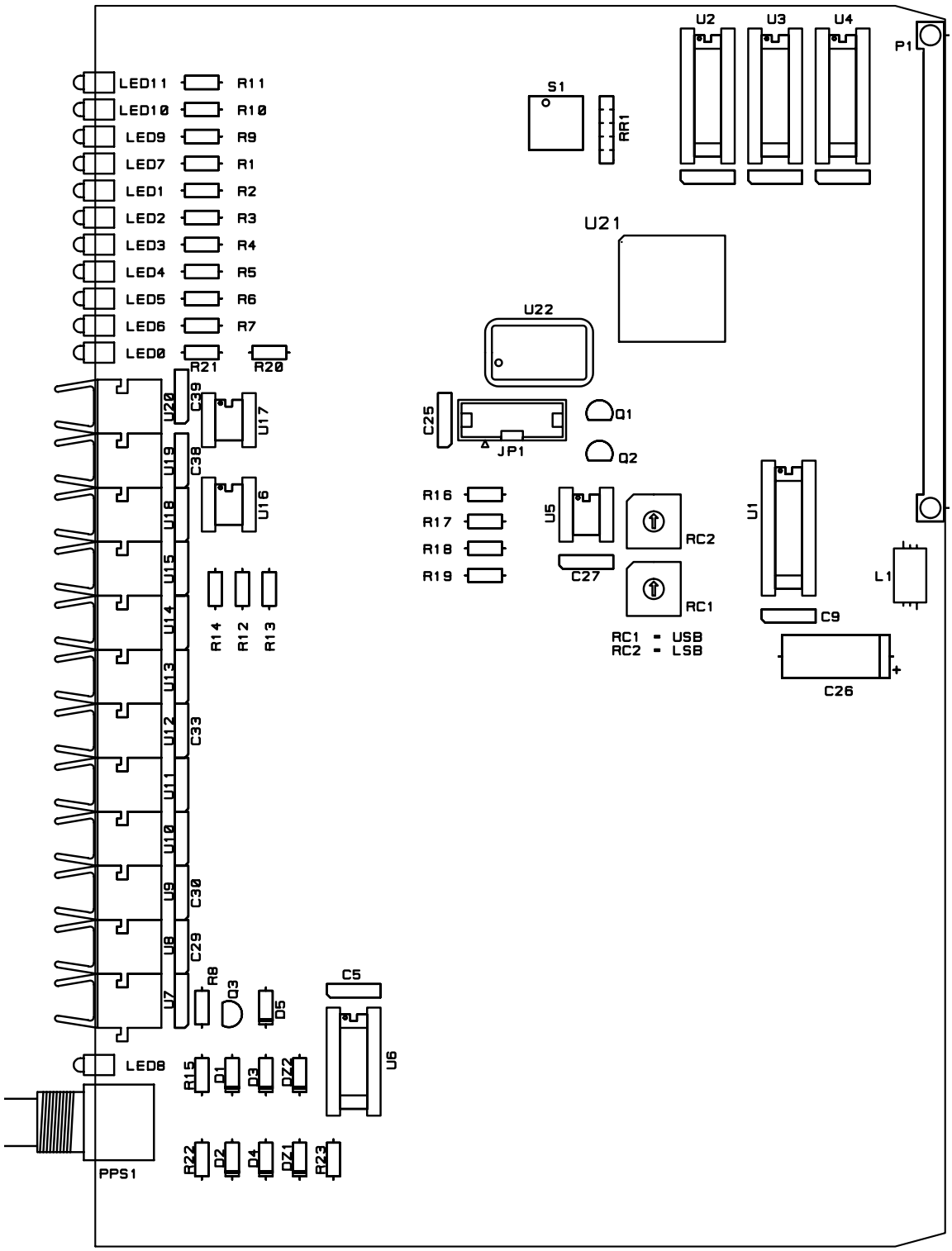
Select Base-Address [A15...A8] using RC1 and RC2.
Select High Nibble [0..F] of the vectors using S1.
Insert the board into the VME crate.
Connect the Receiver's fiber optics
Connect the "TU01" input connector.
Turn on the crate. The yellow "pps" LED should flash at 1 Hz. All red OVF leds also blink if the Status bit ALARM is ON.
Using the debugger:

Write vector OK (Base-Address + 0x1A) Low Nibble (0...F).

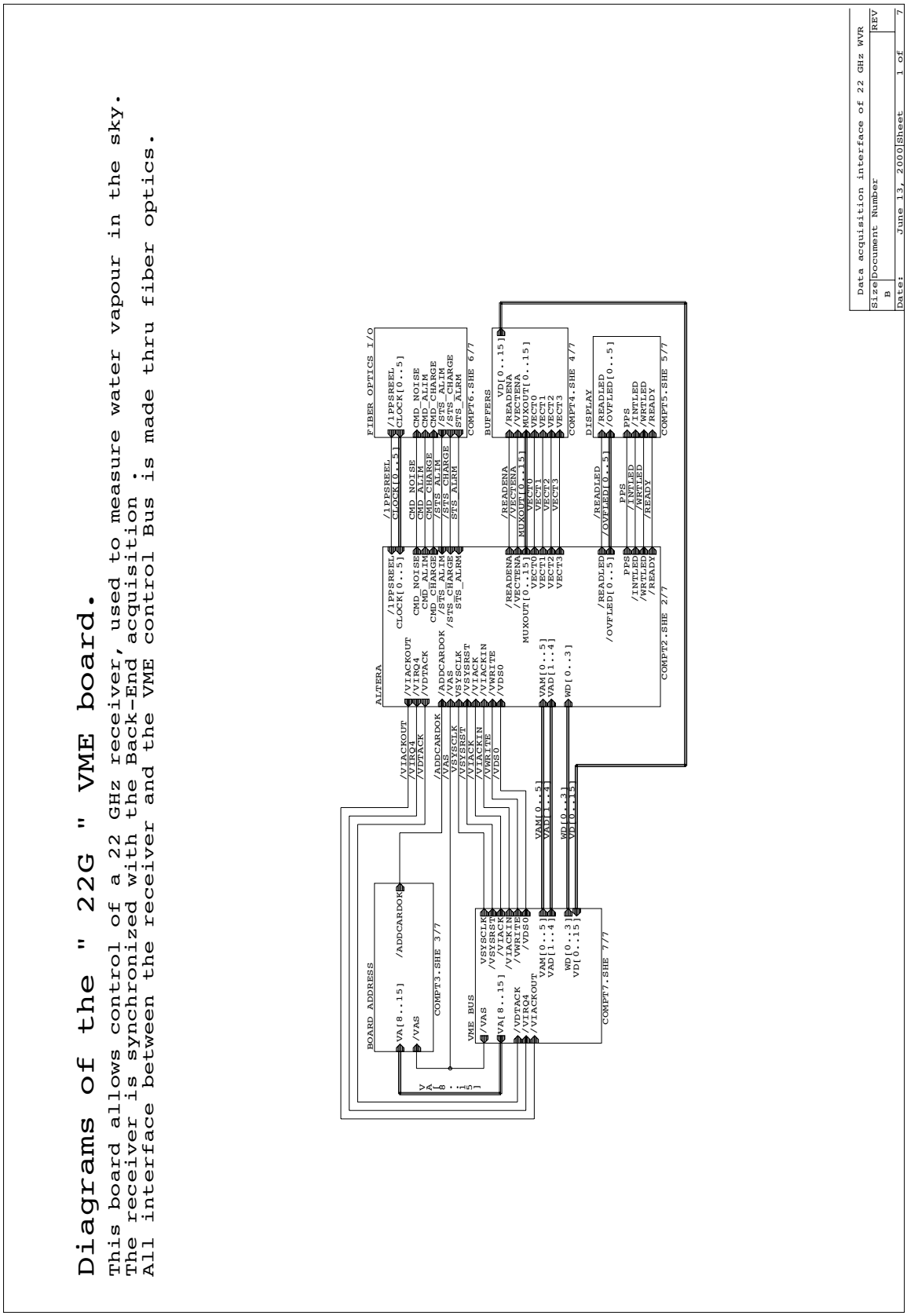
Write vector ERROR (Base-Address + 0x1C) Low Nibble (0...F).

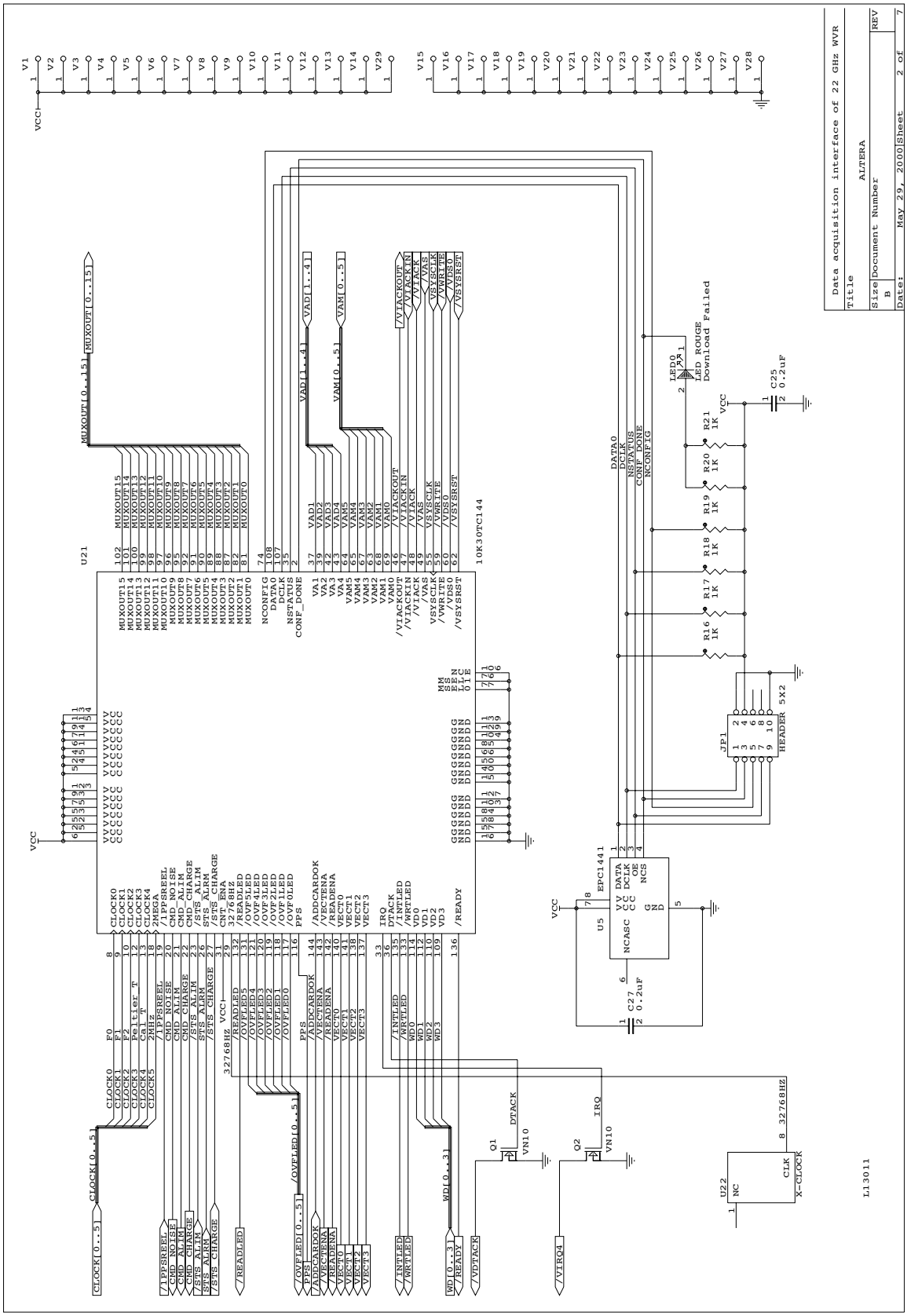
Enable interrupts, writing data "0x8" at (Base-Address + 0x1E): The green LED "READY" should turn ON.

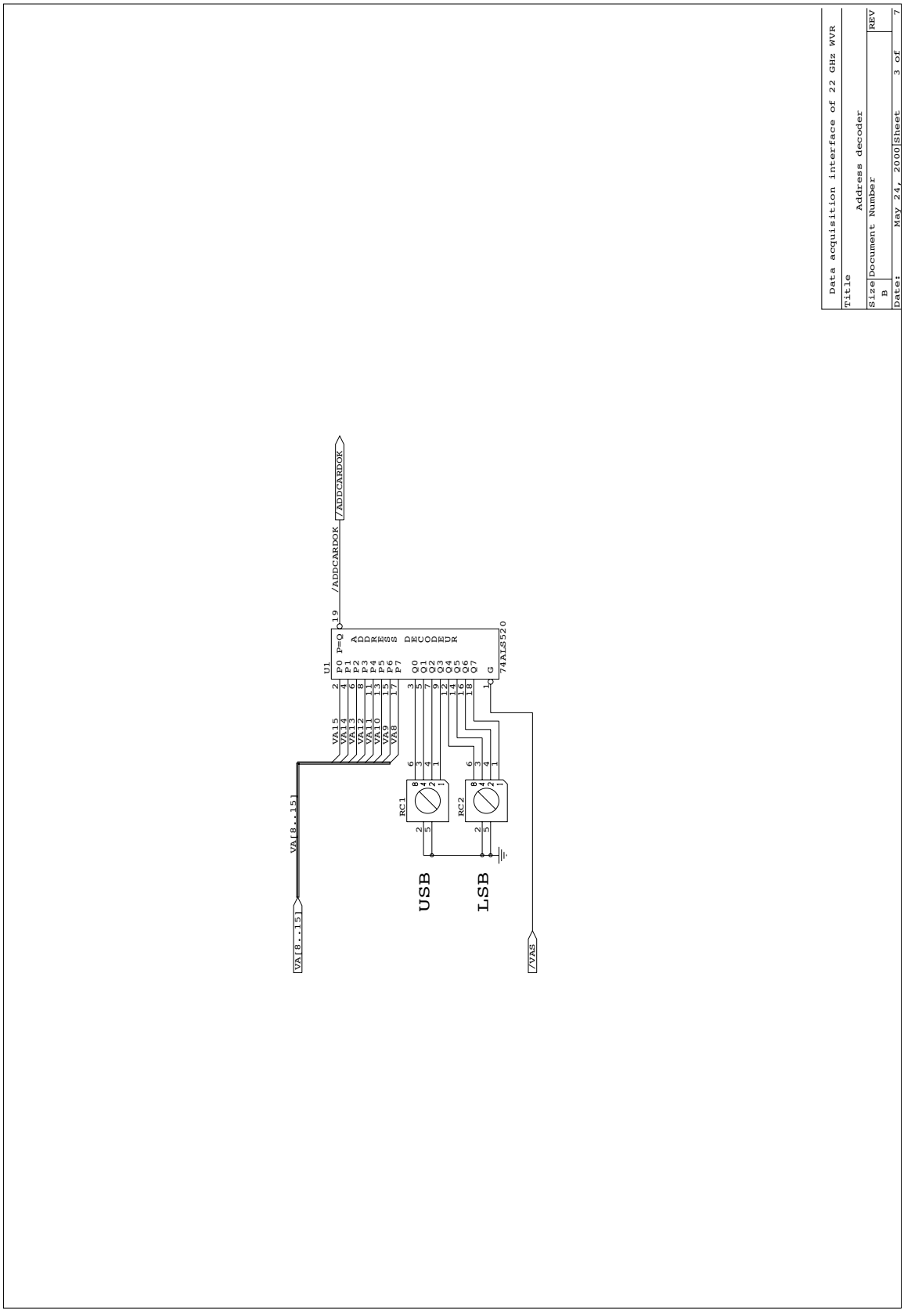
1.12 22G Board layout:

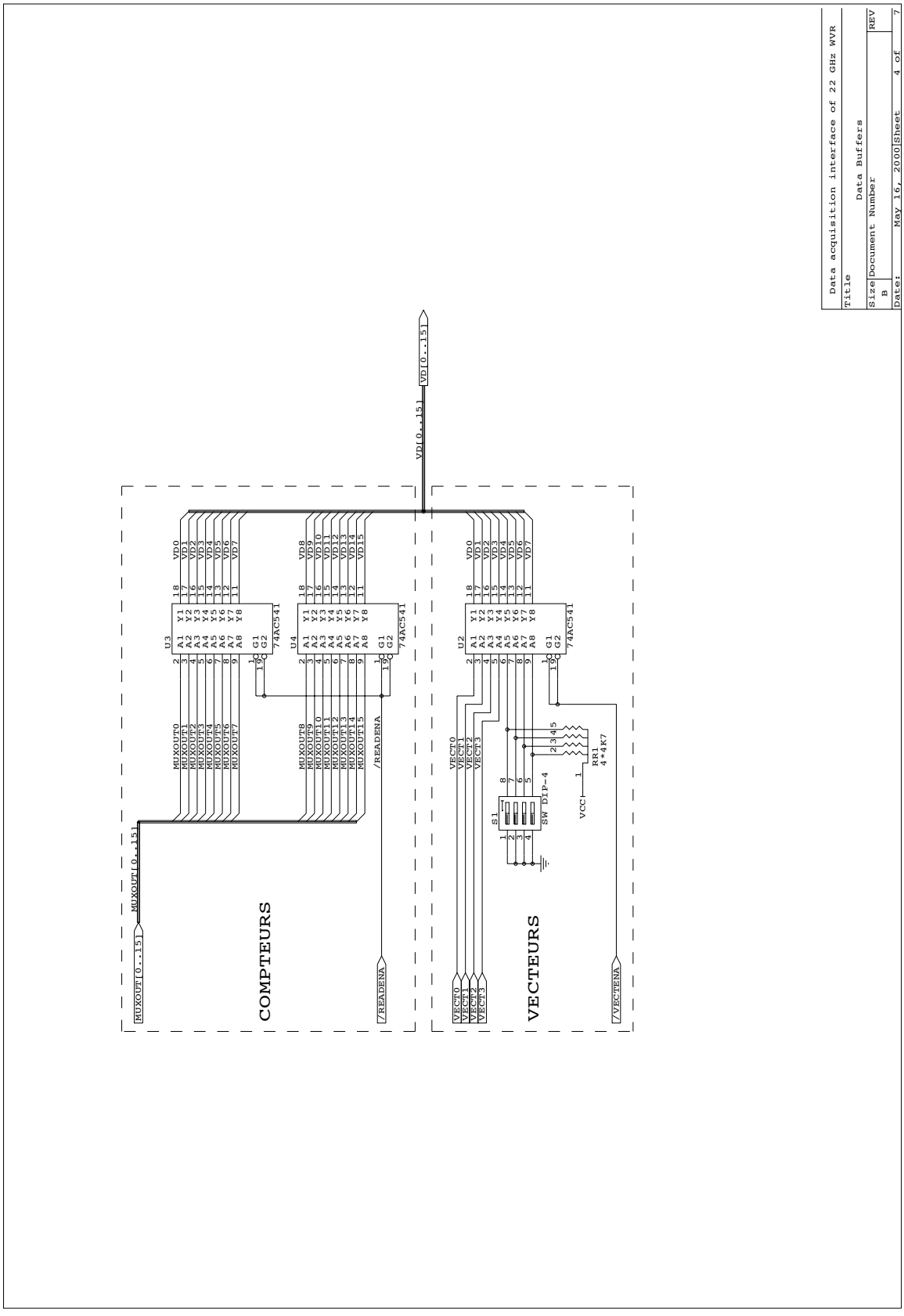


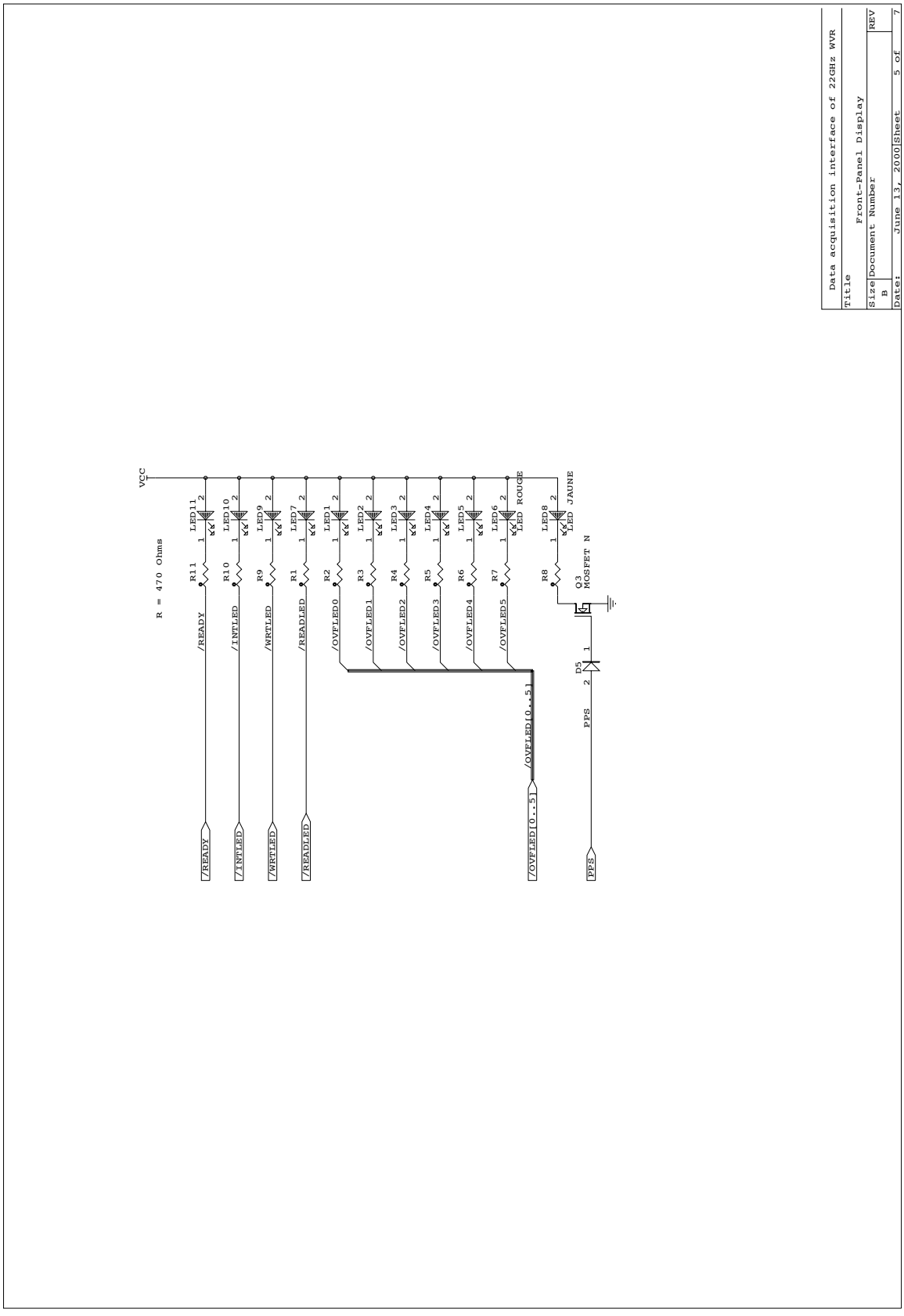
1.13 22G Board schematics:

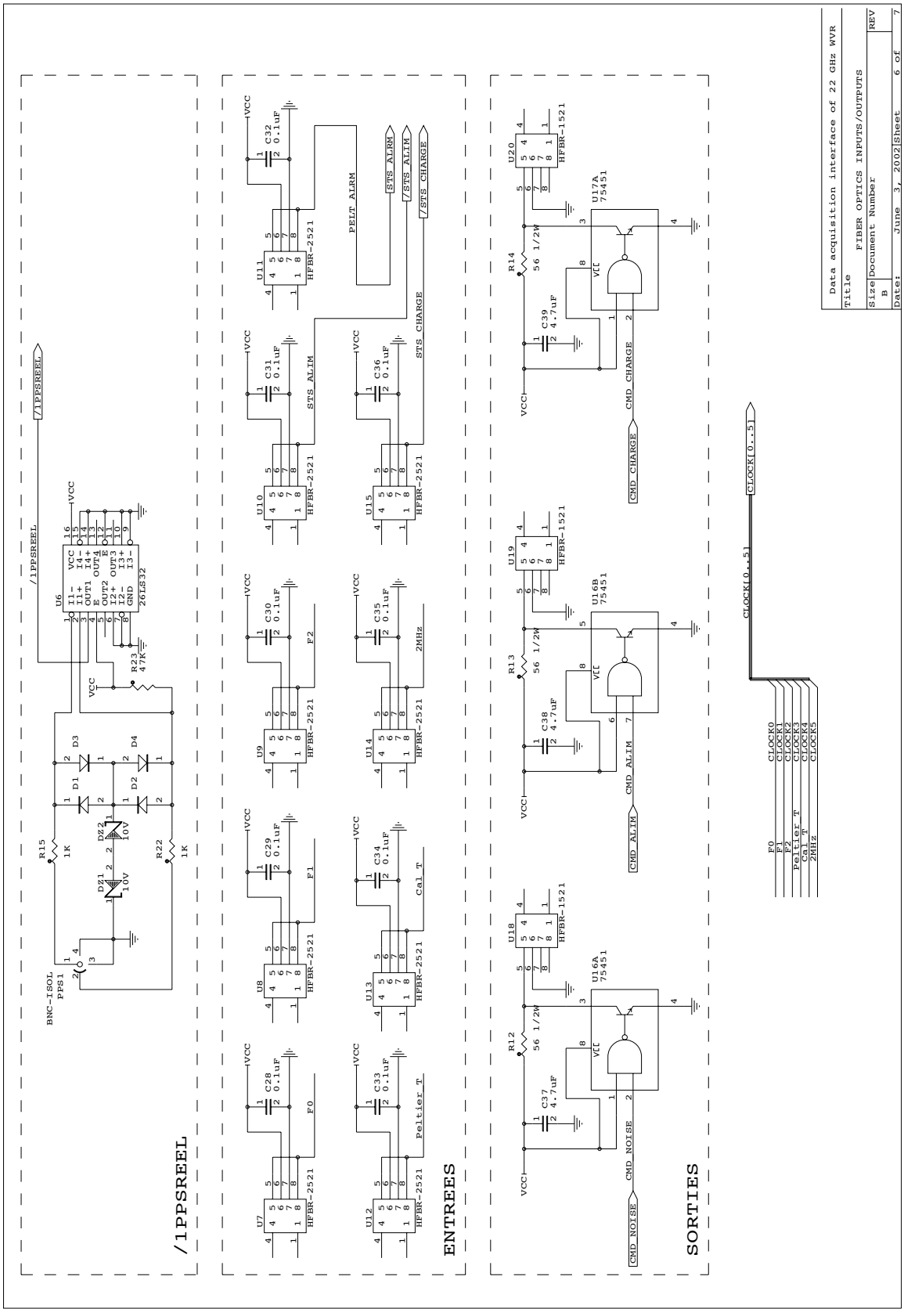


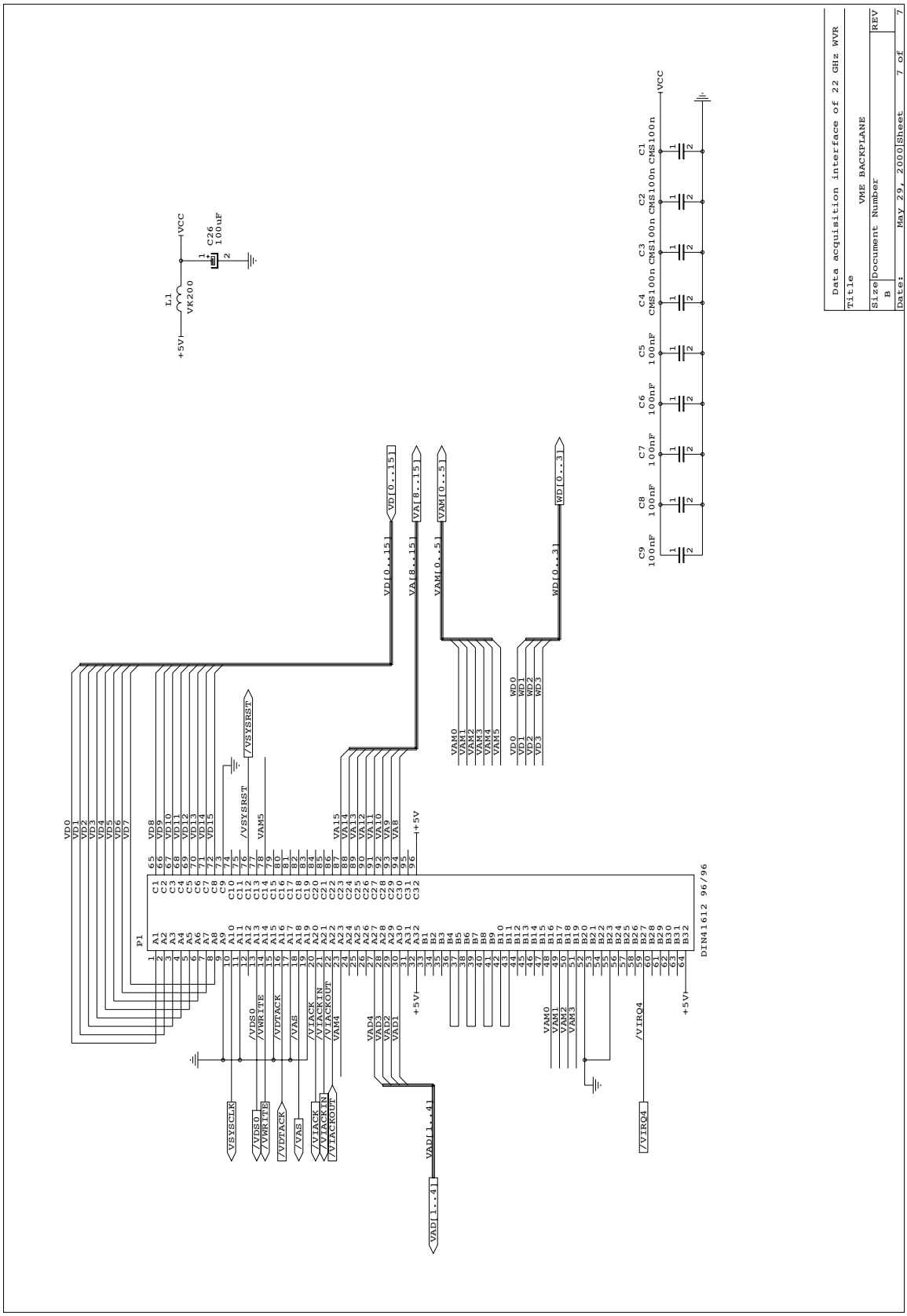

Data acquisition interface of 22 GHz WVR
ALTERA
Size Document Number REV
B
Date: May 29, 2000 Sheet 2 of 7
U21
10K30TC144
U5
EPC1441
U22
JP1
HEADER 5X2
LED3
LED ROUGE
Download Failed
R16 1K
R17 1K
R18 1K
R19 1K
R20 1K
R21 1K
C25 0.2uF
C27 0.2uF
Q1
Q2
VN10
32768HZ
X-CLOCK
MUXOUT[0..15]
VAD[1..41]
VAM[0..5]
CLOCK[0..5]
WD[0..31]
OVFLED[0..5]
DATA0
DCLK
NSTATUS
CONF_DONE
NCONFIG


Data acquisition interface of 22 GHz WVR
Title
Address decoder
Size
B
Document Number
REV
Date: May 24, 2000 Sheet 3 of 7
U1
74ALS520
P0 P=Q
P1
P2
P3
P4
P5
P6
P7
ADDRESS DECODED
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
G
/ADDCARDOK
VA15
VA14
VA13
VA12
VA11
VA10
VA9
VA8
VA[8..15]
RC1
RC2
USB
LSB
/VAS


Data acquisition interface of 22 GHz WVR
Title
Data Buffers
Size
B
Document Number
REV
Date: May 16, 2000 Sheet 4 of 7
VD[0..15]
MUXOUT[0..15]
/READENA
/VECTENA
VECT0
VECT1
VECT2
VECT3
COMPTEURS
VECTEURS
U2
U3
U4
74AC541
SW DIP-4
S1
RR1
4*4K7
VCC


Data acquisition interface of 22GHz WVR
Title
Front-Panel Display
Size B
Document Number
REV
Date: June 13, 2000 Sheet 5 of 7
VCC
R = 470 Ohms
R11
R10
R9
R1
R2
R3
R4
R5
R6
R7
R8
LED11
LED10
LED9
LED7
LED1
LED2
LED3
LED4
LED5
LED6
LED8
LED ROUGE
LED JAUNE
/READY
/INTLED
/WRTLED
/READLED
/OVFLED0
/OVFLED1
/OVFLED2
/OVFLED3
/OVFLED4
/OVFLED5
/OVFLED[0..5]
Q3
MOSFET N
D5
PPS


/1PPSREEL
ENTREES
SORTIES
CLOCK[0..5]
CMD_NOISE
CMD_ALIM
CMD_CHARGE
STS_ALIM
STS_CHARGE
PELT_ALRM
F0
F1
F2
Peltier T
Cal T
2MHz
Data acquisition interface of 22 GHz WVR
FIBER OPTICS INPUTS/OUTPUTS
June 3, 2002


Data acquisition interface of 22 GHz WVR
VME BACKPLANE
Document Number
May 29, 2000
P1
DIN41612 96/96
VD[0..15]
VA[8..15]
VAM[0..5]
WD[0..3]
VAD[1..41]
+5V
VCC
/VSYSRST
/VDS0
/VWRITE
/VDTACK
/VAS
/VIACK
/VIACKIN
/VIACKOUT
/VIRQ4
VSYSCLK
L1
VK200
C26
100uF
C1 CMS100n
C2 CMS100n
C3 CMS100n
C4 CMS100n
C5 100nF
C6 100nF
C7 100nF
C8 100nF
C9 100nF