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E32-DE-IDM-32

Opto-Isolated I/O Board

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1 Description:

This board is used for general purpose I/O. 32 inputs and 32 outputs are available, all of them are opto-isolated.

1.1 Functionalities:

The board is a 6U VME A24/D16 interface. It has interrupt capability (unused on Plateau de Bure). All inputs/outputs are accessible through HE10 40 pos connectors. An iram-made board allows front-panel connections through 2 DIN 64-pos connectors, 1 for inputs and 1 for outputs.
All inputs are isolated from the main ground as well as from any other input.
All outputs are isolated from the main ground as well as from any other output.
The isolation voltage is claimed to be 1000 Volt. This is the value found in the optocoupler datasheet, but for the board itself a value of 48 Volt seems to be more realistic.

1.2 Inputs:

The inputs are TTL compatible, but a limitation resistor is inserted in series with each input. These resistors have a value of 330 Ohms for 5 Volt inputs and 1500 Ohms for 24 Volt inputs. The inputs are polarized and do not accept a reversed polarity.

1.3 Outputs:

The outputs use FET power transistors, driven with opto-generators. The outputs can withstand 50V/1A.
All outputs are passive, but may be made active, using an on-board power supply generated with a DC/DC converter (unused at Bure). The outputs are polarized and do not accept a reversed polarity.

1.4 Using the board:

The board uses a 24-bit address (A24) and 16-bit data (D16). The Address Modifiers (AM) are: 39 , 3D.
It can generate 7 levels of interruption, using 3 different vectors (unused at Bure).
Interrupt levels (IRQ) and vectors are soft-definable.
The Board Base-Address is defined with switches (see below “Switches”).

1.5 Registers:

Address (Hexa)	Read	Write
Base + 0	Auxiliary inputs register	Auxiliary outputs register
Base + 2	Status register	Control register
Base + 8	Grou 0 inputs (J1)	NA
Base + A	Group1 inputs (J2)	NA
Base + C	Reread Group1 outputs	Set Group1 outputs (J4)
Base + E	Reread Group0 outputs	Set Group0 outputs (J3)

1.5.1 Auxiliary outputs registers:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Led3	Led2	Led1	TST	NC	NC	NC	NC	NC	NC	NC	NC	OUT3	OUT2	OUT1	OUT0

D03-D00: Auxiliary outputs, unused.
D12: TST, unused.
D13-D15: Connected to the front-panel Leds. Setting the corresponding bit turns OFF the Led.
Upon power-up, all 3 Leds are ON. In case of a bad FPGA auto-test, only the red Led will turn on.

1.5.2 Auxiliary inputs registers:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Led3	Led2	Led1	TST	NC	NC	NC	NC	NC	NC	NC	NC	IN3	IN2	IN1	IN0

D03-D00: Auxiliary inputs, unused.
D12: TST, unused.
D13-D15: Connected to the front-panel Leds.

1.5.3 Control register:

D15	D14	D13	D12	D11	D10	D09	D08
RES	/PRST	SYS	IRQ1 ENA	IRQ0 ENA	LVL3	LVL2	LVL1

D07	D06	D05	D04	D03	D02	D01	D00
X7	X6	X5	X4	X3	X2	NC	NC

Bits D07-D00 :
Thses bits represent the vector put on the Bus in case of an interrupt generation. D00 will be set automatically if a change has occurred on the group0 inputs, D01 will be set for group1 inputs.

Bits D10-D08:
These bits define the IRQ level used by the board for interrupt generation.

Bits D12-D11:
IRQ0, when set, enables group0 inputs interrupt. IRQ1, when set, enables group1 inputs interrupt. Resetting both bits disables interrupts. These bits **mus**t be reset by software after each interrupt. Handling interrupts on this board is quite uneasy and this option is not used on Plateau de Bure.

Bit D13:
If this bit is reset, the board may be accessed in Supervisor OR User mode (AM = 39 OR 3D). Otherwise, only Supervisor access is possible (AM = 3D).

Bits D15=D14:
Writing one of these bits will write the other one with the same value. To enable the outputs, they **must** be set.

1.5.4 Status register:

Same as the Control register.

1.5.5 Inputs registers:

Reflects the state of group0 inputs and group1 inputs (bit TST of the Control register **must** be reset).

1.5.6 Outputs registers:

The outputs will recopy the contents of these registers (bits RES /PRST of the Control register **must** be set).
The outputs may be reread.

1.6 Original factory I/O connectors (located on the board component side):

	J1	J2	J4	J3
1	Group0 input 1+	Group1 input t 1+	Group1 output t 1+	Group0 output t 1+
2	Group0 input 1-	Group1 input 1-	Group1 output 1-	Group0 output 1-
3	Group0 input 2+	Group1 input 2+	Group1 output 2+	Group0 output 2+
4	Group0 input 2-	Group1 input 2-	Group1 output 2-	Group0 output 2-
5	Group0 input 5+	Group1 input 5+	Group1 output 5+	Group0 output 5+
6	Group0 input 5-	Group1 input 5-	Group1 output 5-	Group0 output 5-
7	Group0 input 6+	Group1 input 6+	Group1 output 6+	Group0 output 6+
8	Group0 input 6-	Group1 input t 6-	Group1 output t 6-	Group0 output t 6-
9	Group0 input 7+	Group1 input 7+	Group1 output 7+	Group0 output 7+
10	Group0 input 7-	Group1 input 7-	Group1 output 7-	Group0 output 7-
11	Group0 input 4+	Group1 input 4+	Group1 output 4+	Group0 output 4+
12	Group0 input 4-	Group1 input 4-	Group1 output 4-	Group0 output 4-
13	Group0 input 3+	Group1 input 3+	Group1 output 3+	Group0 output 3+
14	Group0 input 3-	Group1 input 3-	Group1 output 3-	Group0 output 3-
15	Group0 input 0+	Group1 input 0+	Group1 output 0+	Group0 output 0+
16	Group0 input 0-	Group1 input 0-	Group1 output 0-	Group0 output 0-
17	Group0 input 9+	Group1 input t 9+	Group1 output t 9+	Group0 output t 9+
18	Group0 input 9-	Group1 input 9-	Group1 output 9-	Group0 output 9-
19	Group0 input 10+	Group1 input 10+	Group1 output 10+	Group0 output 10+
20	Group0 input 10-	Group1 input 10-	Group1 output 10-	Group0 output 10-
21	Group0 input 13+	Group1 input 13+	Group1 output 13+	Group0 output 13+
22	Group0 input 13-	Group1 input t 13-	Group1 output t 13-	Group0 output t 13-
23	Group0 input 14+	Group1 input 14+	Group1 output 14+	Group0 output 14+
24	Group0 input 14-	Group1 input t 14-	Group1 output t 14-	Group0 output 14-
25	Group0 input 15+	Group1 input 15+	Group1 output 15+	Group0 output 15+
26	Group0 input 15-	Group1 input 15-	Group1 output 15-	Group0 output 15-
27	Group0 input 12+	Group1 input 12+	Group1 output 12+	Group0 output 12+
28	Group0 input 12-	Group1 input 12-	Group1 output 12-	Group0 output 12-
29	Group0 input 11+	Group1 input 11+	Group1 output 11+	Group0 output 11+
30	Group0 input 11-	Group1 input 11-	Group1 output 11-	Group0 output 11-
31	Group0 input 8+	Group1 input 8+	Group1 output 8+	Group0 output 8+
32	Group0 input 8-	Group1 input 8-	Group1 output 8-	Group0 output 8-

1.7 IRAM I/O connectors:

IRAM developed a piggy-back adaptation board in order to get all inputs on a first connector, all outputs on a second one, both having the same logical and user-friendly pinout and both located on the front-panel.
That way, group0 inputs are referred to as inputs[0-15], group1 inputs as inputs[16-31],
And group0 outputs are referred to as outputs[0-15], group1 outputs as outputs[16-31].

Connector as seen from front-panel:

J5, up most connector:

Pin number (LEFT)	Signal name	Flat cable wire number	Signal name	Pin number (RIGHT)
1	IN0-	1	IN0+	2
3	IN1-	2	IN1+	4

5	IN2-	3	IN2+	6
7	IN3-	4	IN3+	8
9	IN4-	5	IN4+	10
11	IN5-	6	IN5+	12
13	IN6-	7	IN6+	14
15	IN7-	8	IN7+	16
17	IN8-	9	IN8+	18
19	IN9-	10	IN9+	20
21	IN10-	11	IN10+	22
23	IN11-	12	IN11+	24
25	IN12-	13	IN12+	26
27	IN13-	14	IN13+	28
29	IN14-	15	IN14+	30
31	IN15-	16	IN15+	32
33	IN16-	17	IN16+	34
35	IN17-	18	IN17+	36
37	IN18-	19	IN18+	38
39	IN19-	20	IN19+	40
41	IN20-	21	IN20+	42
43	IN21-	22	IN21+	44
45	IN22-	23	IN22+	46
47	IN23-	24	IN23+	48
49	IN24-	25	IN24+	50
51	IN25-	26	IN25+	52
53	IN26-	27	IN26+	54
55	IN27-	28	IN27+	56
57	IN28-	29	IN28+	58
59	IN29-	30	IN29+	60
61	IN30-	31	IN30+	62
63	IN31-	32	IN31+	64

J6, bottom connector:

Pin number (LEFT)	Signal name	Flat cable wire number	Signal name	Pin number (RIGHT)
1	OUT0-	1	OUT0+	2
3	OUT1-	2	OUT1+	4
5	OUT2-	3	OUT2+	6
7	OUT3-	4	OUT3+	8
9	OUT4-	5	OUT4+	10
11	OUT5-	6	OUT5+	12
13	OUT6-	7	OUT6+	14
15	OUT7-	8	OUT7+	16
17	OUT8-	9	OUT8+	18
19	OUT9-	10	OUT9+	20
21	OUT10-	11	OUT10+	22
23	OUT11-	12	OUT11+	24
25	OUT12-	13	OUT12+	26
27	OUT13-	14	OUT13+	28
29	OUT14-	15	OUT14+	30
31	OUT15-	16	OUT15+	32
33	OUT16-	17	OUT16+	34
35	OUT17-	18	OUT17+	36
37	OUT18-	19	OUT18+	38
39	OUT19-	20	OUT19+	40
41	OUT20-	21	OUT20+	42
43	OUT21-	22	OUT21+	44
45	OUT22-	23	OUT22+	46

47	OUT23-	24	OUT23+	48
49	OUT24-	25	OUT24+	50
51	OUT25-	26	OUT25+	52
53	OUT26-	27	OUT26+	54
55	OUT27-	28	OUT27+	56
57	OUT28-	29	OUT28+	58
59	OUT29-	30	OUT29+	60
61	OUT30-	31	OUT30+	62
63	OUT31-	32	OUT31+	64

1.8 Conclusion:

The I/O boards are used at Plateau de Bure in minimum configuration. Certain options are unusable (interrupts), suppressed (function TST which introduced erratic spikes), or modified (input GALs 22V10 replaced with GALs 6001 containing simpler equations, I/O connectors).