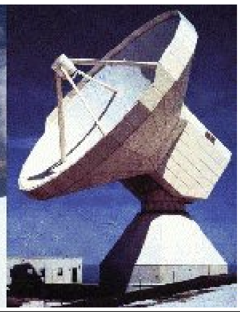

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SubRef VME Board

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Keywords:

Approved by:	Date:	Signature:
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Change Record

REVISION	DATE	AUTHOR	SECTION/PAGE AFFECTED	REMARKS
1	July 8 2004	Francis Morel		

Contents

1 SUBREF VME Board description

This board is a slave device, under control of a remote microprocessor.
This board was designed for Subreflector control. The subreflector hyperbolic mirror needs dynamic correction to compensate for the main mirror deformation under gravity, depending on the antenna elevation. Tilt, translations and focus adjustments are also necessary.
The Subref board drives 5 motors, moving the mirror as requested by the microprocessor. The Subref board is composed of a carrier board in charge of the VME Bus interface, and 5 similar daughter "Submot" boards, each "Submot" driving one motor.
The motors are powered and connected to the Submot boards through an electronic rack, which also provides an optical isolation. This is the rack "SubIsol", which is not described in this documentation.

1.1 Motors and associated logics:

The 5 motors (mot1 to mot5) are similar. Each of them is a DC motor equipped with an encoder delivering 100 periods of a Sine/Cosine TTL signal per motor revolution. The encoder does not supply any reference pulse. The impulsions of the encoder are subdivided by 64 in the electronics, which allows counting the motor revolutions with a resolution of 64/100 (originally 1) revolution.
Each motor is equipped with a precision microswitch. A bit of the Status register (SWI[x]) reflects the state of this switch: SWI[x] = 0 when motor[x] is positioned in the normal displacement zone, and SWI[x] = 1 when motor[x] has reached its stroke limit in negative direction. The switch is also used as a hardware limit switch and SWI[x] = 1 will forbid motor[x] moves with negative velocity.
The Subref board allows reading the actual position (16-bit signed APOS signed registers) and setting the requested position (16-bit RPOS signed registers) and requested velocity of each motor. Setting a velocity request bit (PVR[x] or NVR[x] of the CMR, x being the motor number [1..5]) forces the selected motor to move with requested constant velocity. A move towards the switch has negative velocity. A velocity request is always effective.
For position control, the motor position has to be initialized first. This is done through the 16-bit Command register (CMR) and checked through the 16-bit Status register (STS) of the Subref board.

Command Register (CMR):

15	14	13	12	11	10	09	08	07	060	05	04	03	02	01	00
TST	NVR5	PVR5	ENA5	NVR4	PVR4	ENA4	NVR3	PVR3	ENA3	NVR2	PVR2	ENA2	NVR1	PVR1	ENA1

TST: May be set/reset (for tests only).
NVR[x]: forces motor[x] to move with constant negative velocity.
PVR[x]: forces motor[x] to move with constant positive velocity.
ENA[x]: If ID[x] = 0, ENA[x] preloads motor[x] position register to zero, upon transition (from 0 to 1) of SWI[x]. Bit ID[x] of Status is then set. Resetting ENA[x] resets ID[x].

Status Register (STS):

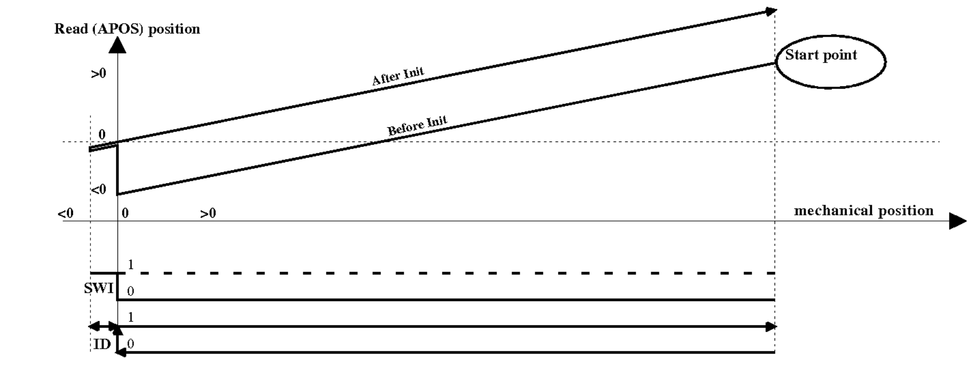
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TST	RUN5	ID5	SWI5	RUN4	ID4	SWI4	RUN3	ID3	SWI3	RUN2	ID2	SWI2	RUN1	ID1	SWI1

TST: recopy of bit TST of the CMR.
RUN[x]: motor[x] is requested to move, in any way.
ID[x]: Init Done[x] = 1 when motor[x] has been initialized.
SWI[x]: Switch of motor[x], set if motor[x] has reached its negative limit.

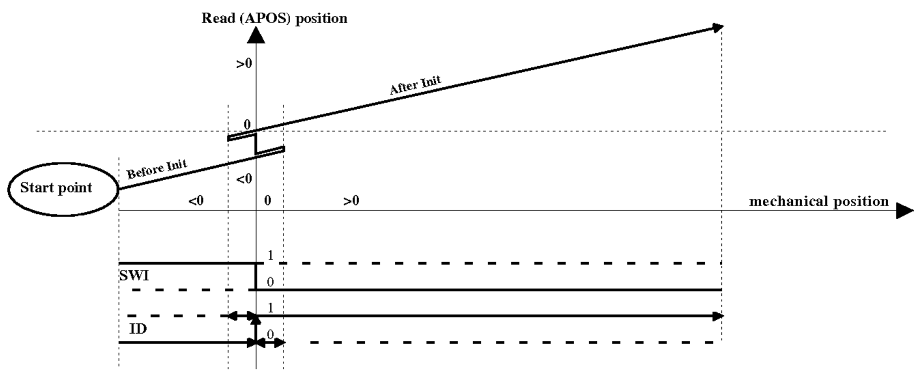
1.2 Motors' init:

Upon turn-on, the actual position of a motor is unknown, as it is not initialized. For initialization, following commands are used:
-SWI[x] is checked first:
If SWI[x] = 1, PVR[x] is set, forcing motor[x] to run at constant velocity in the positive direction, until SWI[x] = 0. The motor stops, PVR[x] is then reset.

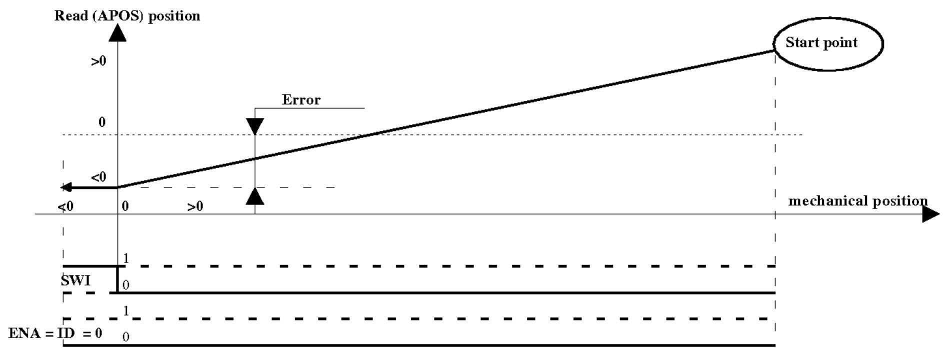
-If SWI = 0, NVR[x] and ENA[x] are set, forcing motor[x] to move with constant negative velocity until SWI[x] = 1. Upon SWI[x] transition (from 0 to 1), the board preloads APOS[x] register to 0x0000 and sets ID[x]. The motor stops, it is now initialized.
-Resetting NVR[x] will set motor[x] in position control mode.



SUBREF: Motor position Init (starting with SWI = 0)



SUBREF: Motor position Init (starting with SWI = 1)



SUBREF: Checking motor position reliability (Error should be zero)

1.3 Position control mode:

Once in this mode, motor[x] will go to the requested position. This position value is writable in the Requested Position Register, RPOS[x]. The actual position is readable in the Actual Position Register (APOS[x]). As might be expected, a move with negative velocity (move down) will decrease the position value. Positive velocity (move up) move will increase it.

1.4 Caveat user:

-Upon turn-on, all bits of the CMR are reset. Thus, ID[x] of the Status are reset. All bits of APOS[x] and RPOS[x] registers are also reset.
-A VME "Reset" has **NO** effect on the board.
-Bits PVR[x] and NVR[x] are mutually exclusive and if both are set, motor[x] always stops.
-Setting PVR[x] = 1 and NVR[x] = 0 causes motor[x] to move at constant positive velocity.
-Setting PVR[x] = 0 and NVR[x] = 1 causes motor[x] to move at constant negative velocity.
-When NVR[x] = 0 AND PVR[x] = 0 AND **ID[x] = 1,** motor[x] will always go to RPOS[x] position.
-If ENA[x] = 0, SWI[x] transition (from 0 to 1) will NOT preload APOS[x] to zero, but will "freeze" the contents of APOS[x]. This sampling is used for checking the reproducibility of position "zero".

1.5 VME interface:

The board is a A16/D16 standard VME board. It is mapped in the VME 16-bit "short" address space.
All register addresses are relative to the Base Address selected with the encoding wheels **RC2(A15-A12)** and **RC1(A11-A8)**.
-The actual address on Plateau de Bure of the Subref Board is 0xFFFFFE00.

Register name	Register address	Data
STS	0x00	Status register (Read only)
APOS1	0x04	Actual Position of Motor1 (Read only)
APOS2	0x08	Actual Position of Motor2 (Read only)
APOS3	0x0C	Actual Position of Motor3 (Read only)
APOS4	0x10	Actual Position of Motor4 (Read only)
APOS5	0x14	Actual Position of Motor5 (Read only)
CMR	0x00	Command Register (Write only)
RPOS1	0x04	Requested Position of Motor1 (Write only)
RPOS2	0x08	Requested Position of Motor2 (Write only)
RPOS3	0x0C	Requested Position of Motor3 (Write only)
RPOS4	0x10	Requested Position of Motor4 (Write only)
RPOS5	0x14	Requested Position of Motor5 (Write only)

1.6 Switches, jumpers:

-Subref Base Address (address bits [A15…A8]) is selectable using 2 rotary encoding wheels on the board.

Encoding wheel	VME address bits
RC2 (0 to F)	A15..A12
RC1 (0 to F)	A11..A8

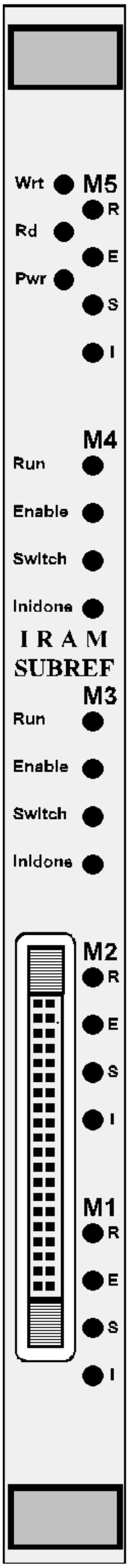
-Each Submot board samples the encoders' signals; it detects, filters and counts the rotations. The sample frequency is selectable with **jumper SK1 on a 16-pin DIP socket**:

Jumper SK1 position	Sampling frequency
1-16	4 MHz
2-15	2 MHz
3-14	1 MHz

4-13	500 kHz
5-12	**250 kHz (default)**
6-11	125 kHz
7-10	62.5 kHz
8-9	31.25 kHz

This adjustment depends on the complete (motor + encoder + logics) configuration, and should not be modified.

1.7 SUBREF Board Front-Panel:



1.8 Front-panel display:

The main carrier board, as well as the Submot boards uses FPGA chips. This allows easy modification of the functions. This also guarantees the short response times necessary for real-time motors driving.

The carrier board is in charge of the VME transactions. It drives 3 LEDs, displaying VME access and power status.

Each Submot drives 4 LEDs: Visible on the front-panel as 5 groups of 4 LEDs , they allow knowing at a glance the status of each motor.

LED name	Led colour	LED function
Wrt	Yellow	VME Write access display
Rd	Yellow	VME Read access display
Pwr	Green	VME Power On display
Run (Mx)	Yellow	RUN[x] display
Enable(Mx)	Green	ENA[x] display
Switch(Mx)	Red	SWI[x] display
Inidone(Mx)	Green	ID[x] display

1.9 Front-panel connector:

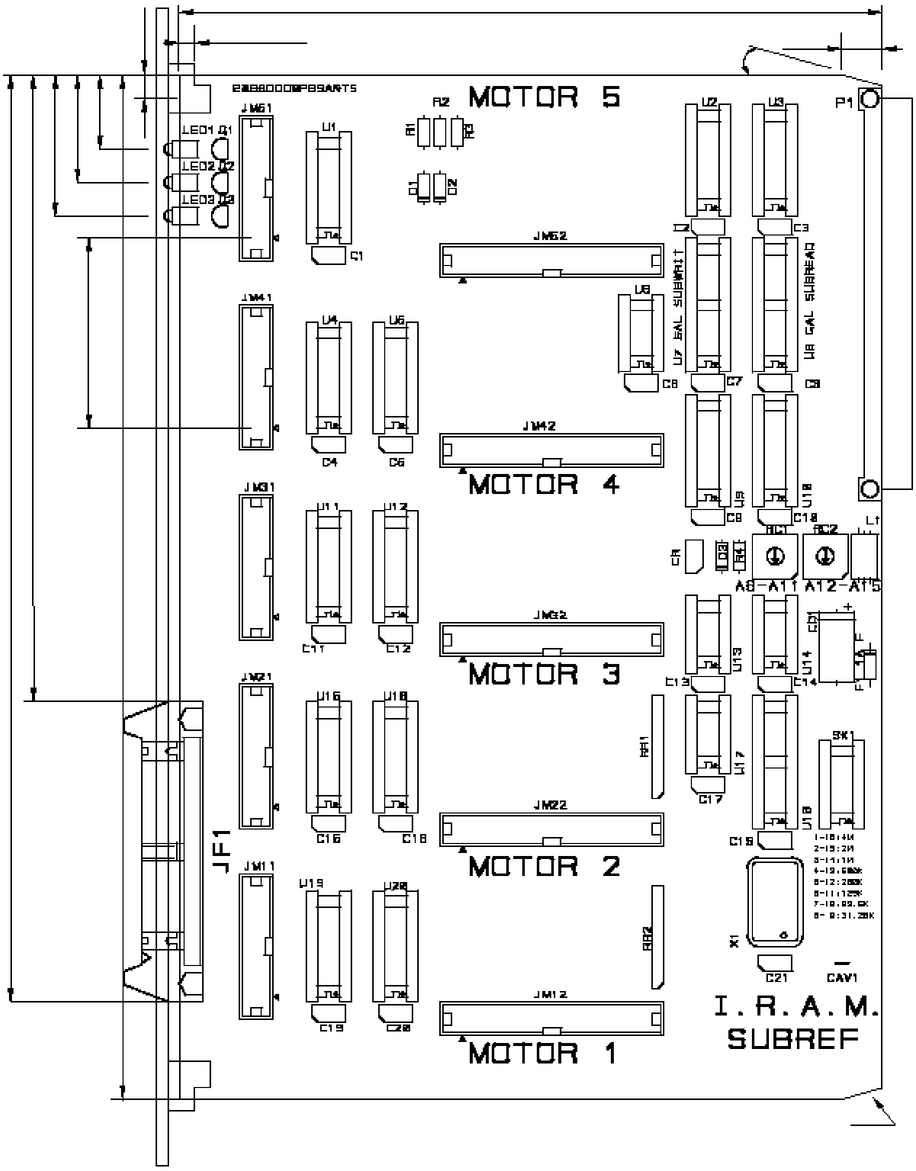
Connections between the Subref board and the SubIsol rack are made through a 40-pos flat cable. All are TTL signals. Each motor needs 5 signals:

Signal name	Signal direction (as viewed from VME)	
INSIN[x]	Input	Motor[x] encoder SIN signal
INCOS[x]	Input	Motor[x] encoder COS signal
/INSWI[x]	Input	Motor[x] switch: 0 Volt when TRUE
OUTUP[x]	Output	Motor[x] “Move Up” command
OUTDN[x]	Output	Motor[x] “Move Down” command

Pinout of the front-panel connector:

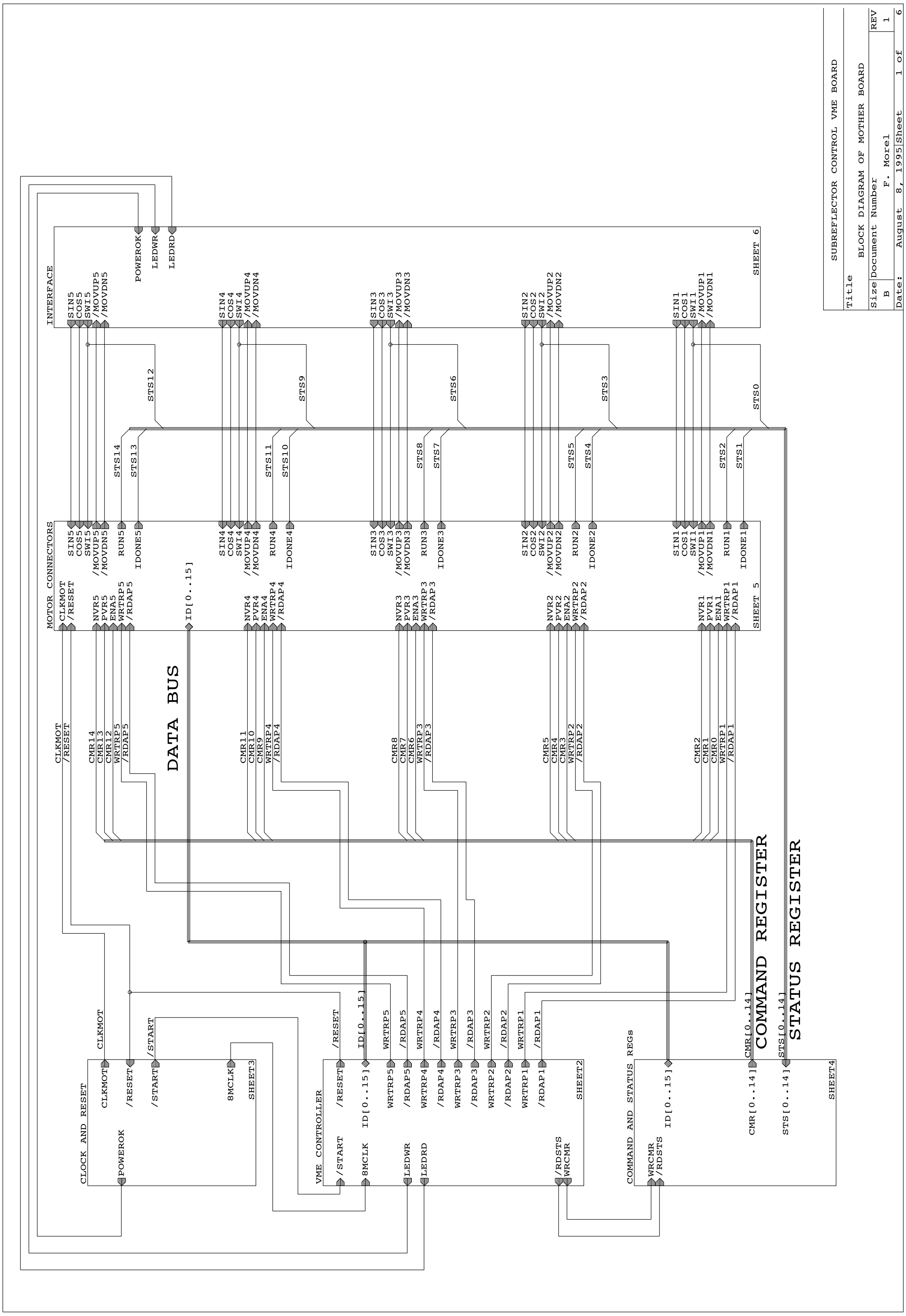
Pin	Signal Name	Comments	Pin	Signal name	Comments
1	+5V Out	Fuse protected	2	+5V Out	Fuse protected
3	+5V Out	Fuse protected	4	+5V Out	Fuse protected
5	+5V Out	Fuse protected	6	+5V Out	Fuse protected
7	+5V Out	Fuse protected	8	+5V Out	Fuse protected
9			10	GND	
11	INSIN1	TTL input	12	INCOS1	TTL input
13	/INSWI1	LOW when switch ON	14	OUTUP1	TTL output
15	OUTDN1	TTL output	16	GND	
17	INSIN2	TTL input	18	INCOS2	TTL input
19	/INSWI3	LOW when switch ON	20	OUTUP2	TTL output
21	OUTDN4	TTL output	22	GND	
23	INSIN3	TTL input	24	INCOS3	TTL input
25	/INSWI3	LOW when switch ON	26	OUTUP3	TTL output
27	OUTDN3	TTL output	28	GND	
29	INSIN4	TTL input	30	INCOS4	TTL input
31	/INSWI4	LOW when switch ON	32	OUTUP4	TTL output
33	OUTDN4	TTL output	34	GND	
35	INSIN5	TTL input	36	INCOS5	TTL input
37	/INSWI5	LOW when switch ON	38	OUTUP5	TTL output
39	OUTDN5	TTL output	40	GND	

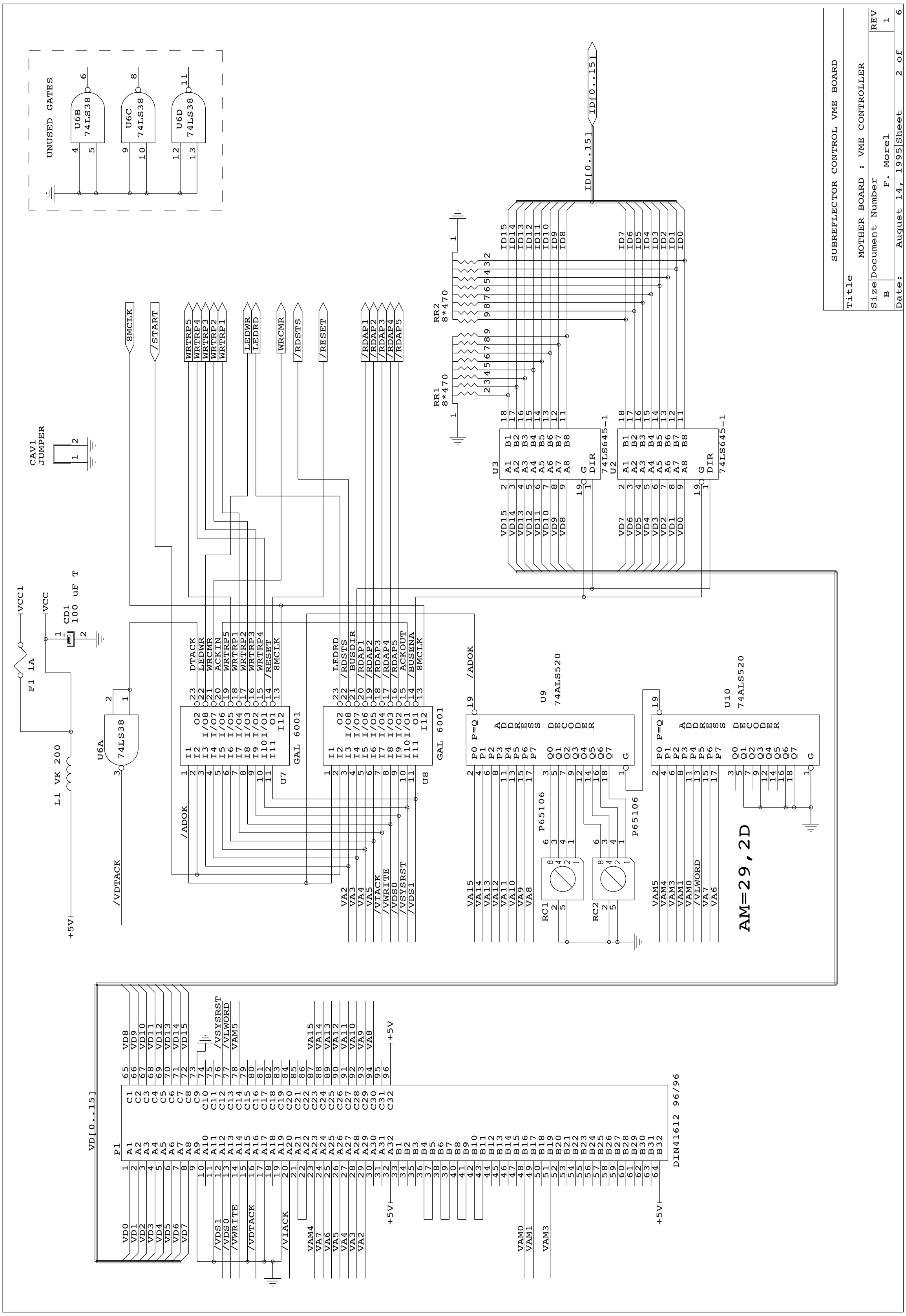
1.10 Subref Board layout:

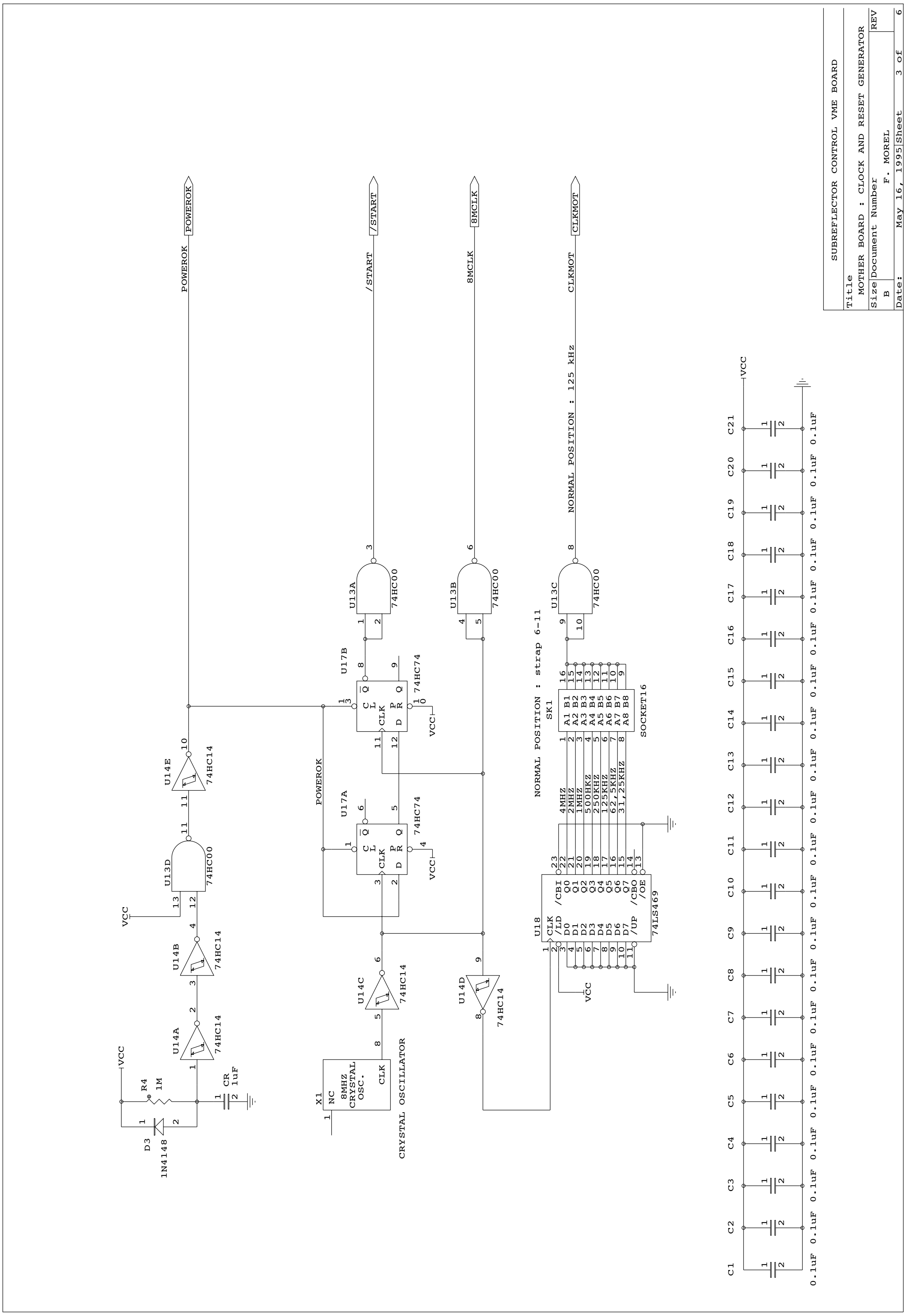


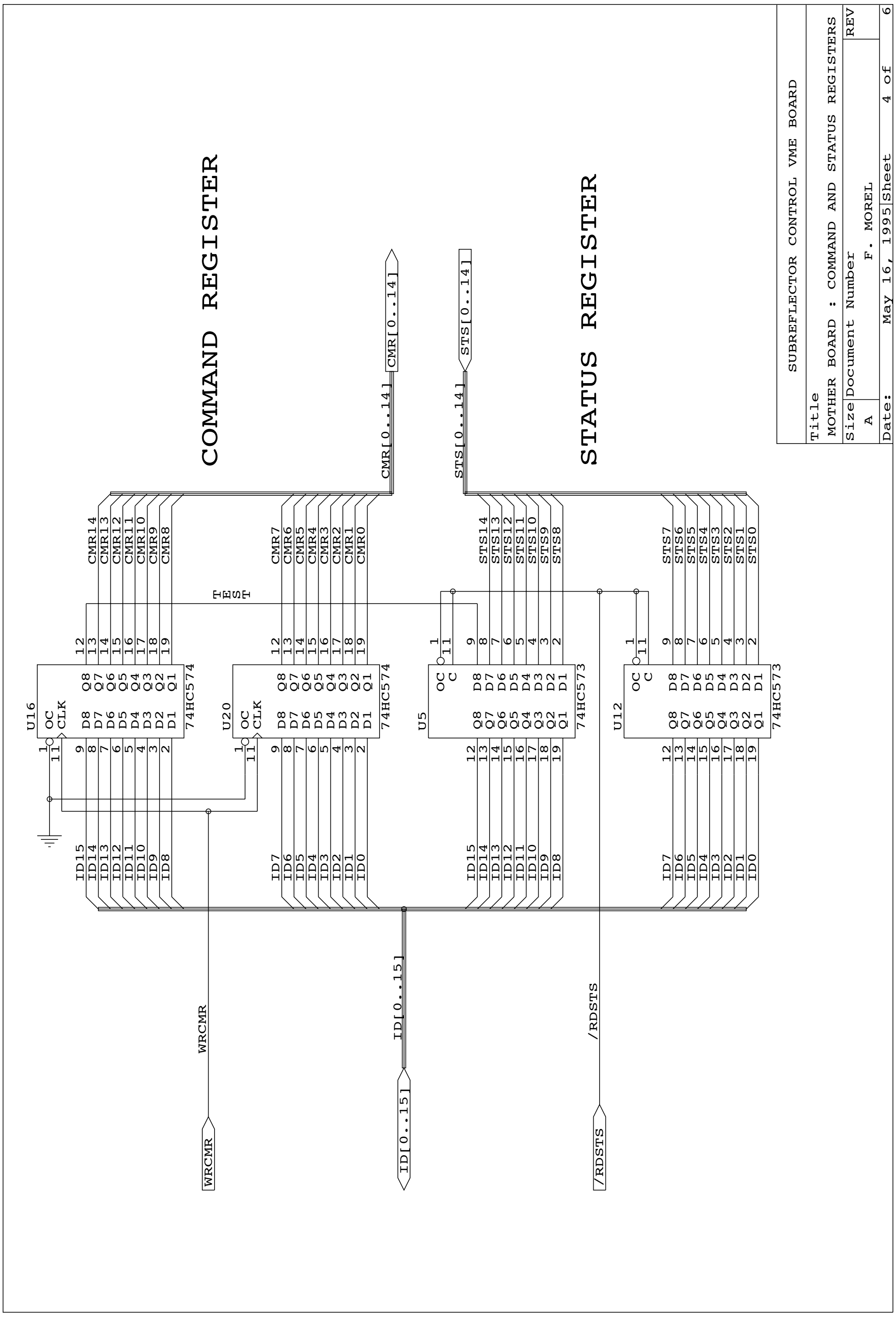
N.B: *as seen with the 5 Submot boards removed*

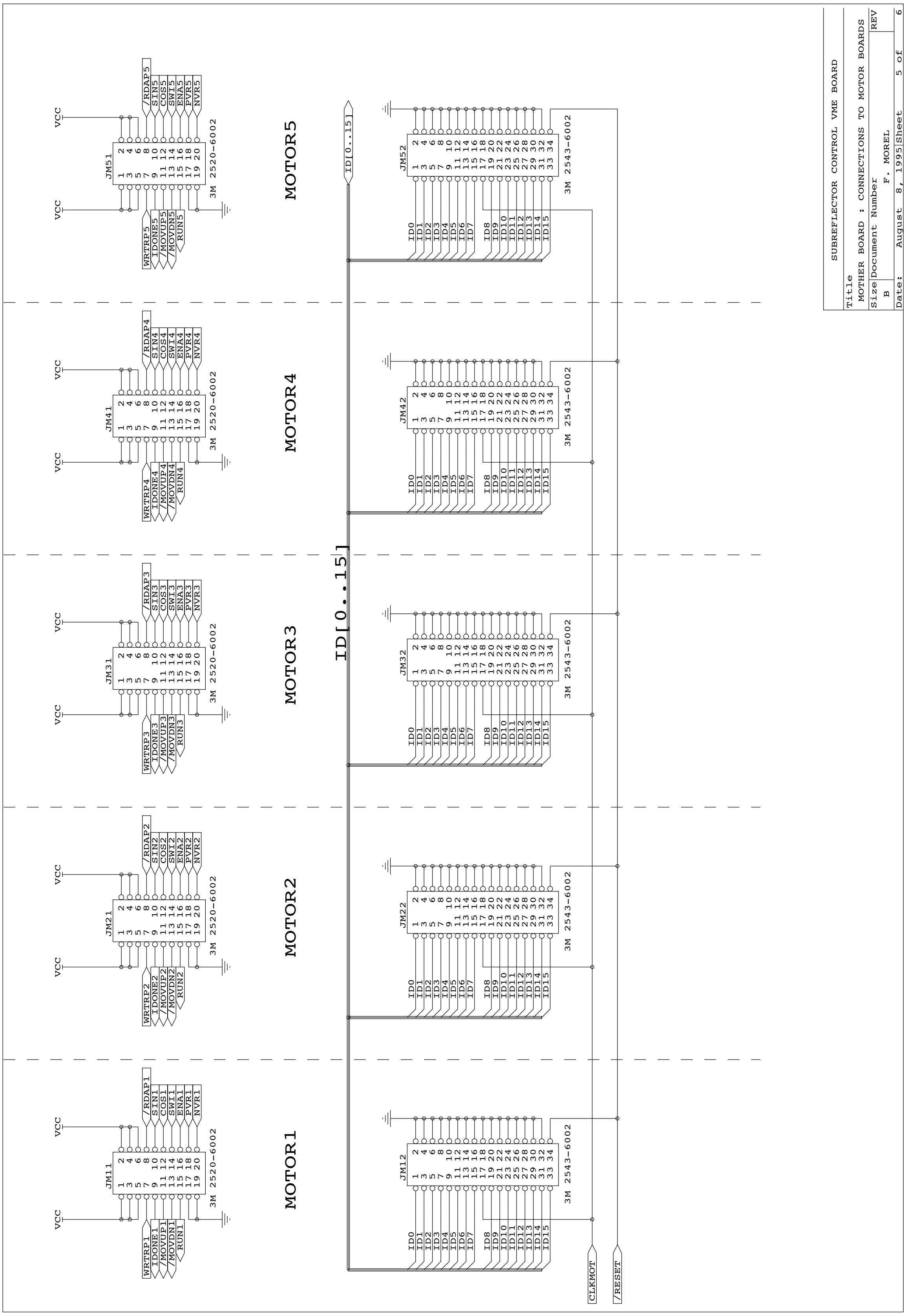
1.11 Subref Board schematics:

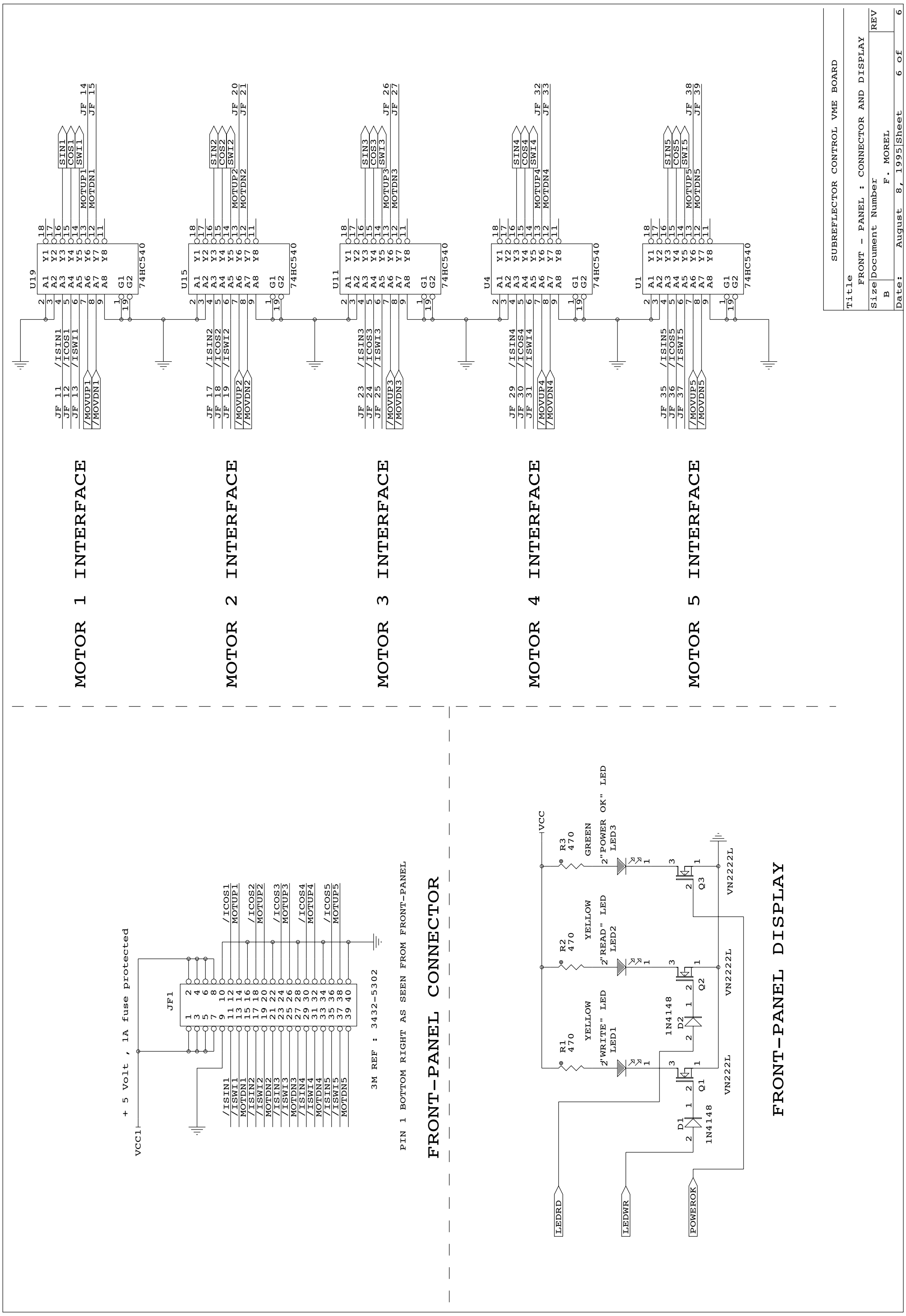



SUBREFLECTOR CONTROL VME BOARD
MOTHER BOARD : VME CONTROLLER
F. Morel
August 14, 1995
UNUSED GATES
AM=29,2D

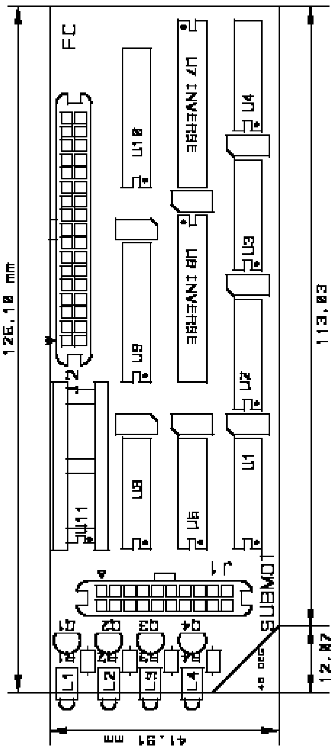

SUBREFLECTOR CONTROL VME BOARD
Title
MOTHER BOARD : CLOCK AND RESET GENERATOR
Size Document Number REV
B F. MOREL
Date: May 16, 1995 Sheet 3 of 6
POWEROK
/START
8MCLK
CLKMOT
NORMAL POSITION : 125 kHz
NORMAL POSITION : strap 6-11
SK1
SOCKET16
4MHZ
2MHZ
1MHZ
500HKZ
250KHZ
125KHZ
62,5KHZ
31,25KHZ
U18
74LS469
U13A 74HC00
U13B 74HC00
U13C 74HC00
U13D 74HC00
U14A 74HC14
U14B 74HC14
U14C 74HC14
U14D 74HC14
U14E 74HC14
U17A 74HC74
U17B 74HC74
X1
NC
8MHZ CRYSTAL OSC.
CLK
CRYSTAL OSCILLATOR
R4 1M
D3 1N4148
CR 1uF
VCC
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21
0.1uF


COMMAND REGISTER
STATUS REGISTER
CMR[0..14]
STS[0..14]
ID[0..15]
WRCMR
/RDSTS
TEST
U16
U20
U5
U12
74HC574
74HC573
SUBREFLECTOR CONTROL VME BOARD
Title
MOTHER BOARD : COMMAND AND STATUS REGISTERS
Size Document Number
A F. MOREL
REV
Date: May 16, 1995 Sheet 4 of 6

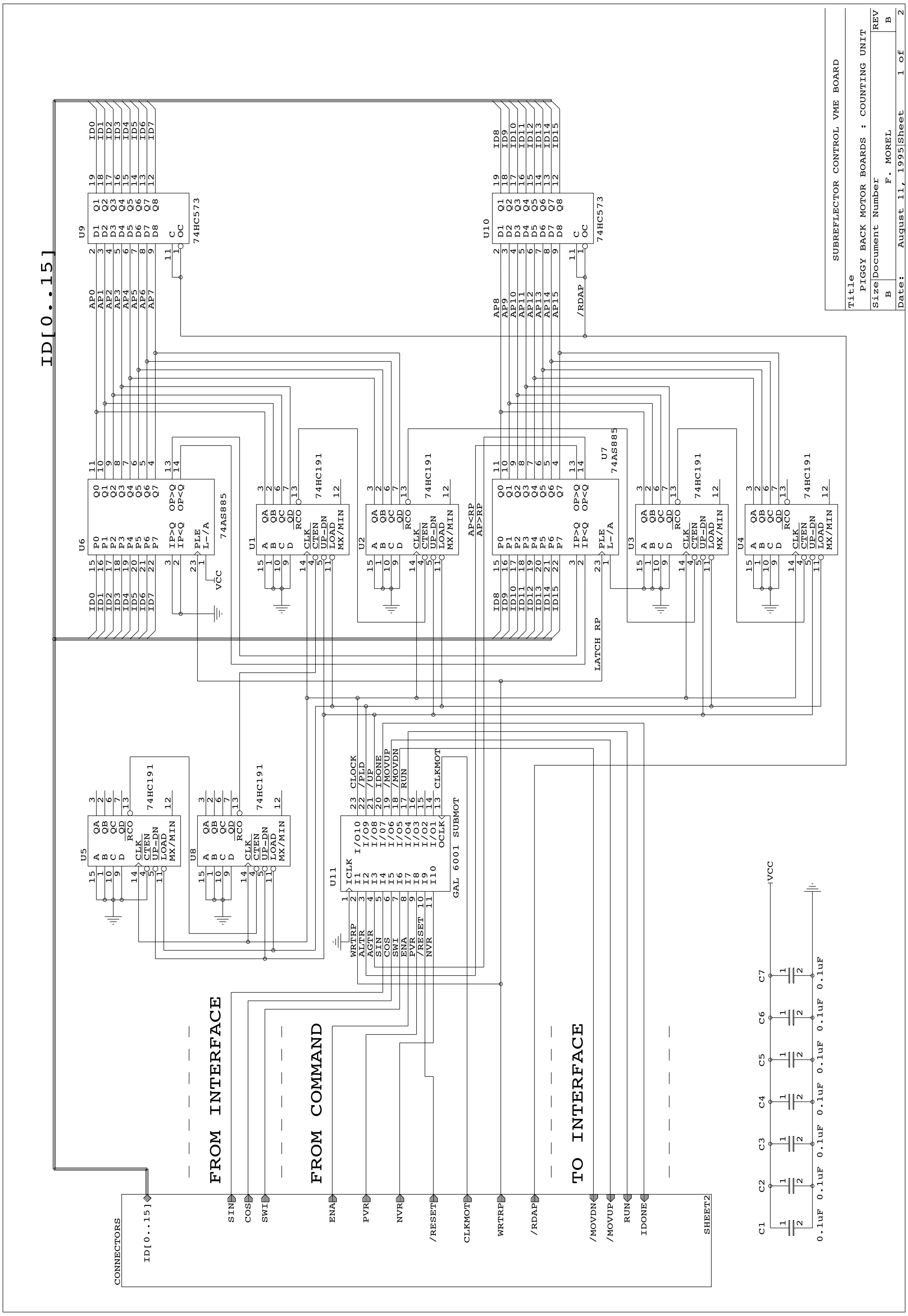

SUBREFLECTOR CONTROL VME BOARD
Title
MOTHER BOARD : CONNECTIONS TO MOTOR BOARDS
Size Document Number REV
B F. MOREL
Date: August 8, 1995 Sheet 5 of 6
MOTOR1
MOTOR2
MOTOR3
MOTOR4
MOTOR5
ID[0..15]
CLKMOT
/RESET
3M 2520-6002
3M 2543-6002

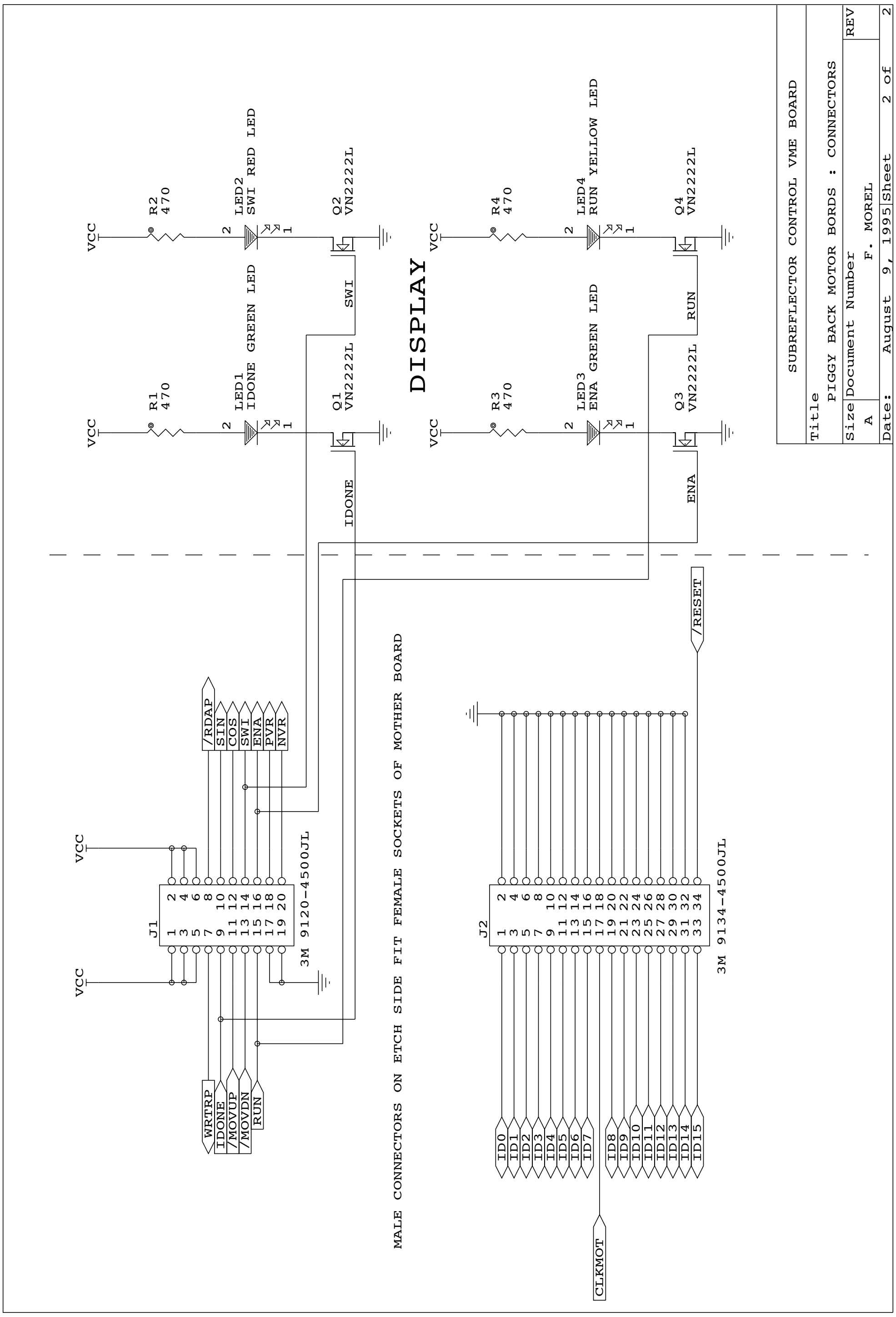

MOTOR 1 INTERFACE
MOTOR 2 INTERFACE
MOTOR 3 INTERFACE
MOTOR 4 INTERFACE
MOTOR 5 INTERFACE
74HC540
+ 5 Volt , 1A fuse protected
JF1
3M REF : 3432-5302
PIN 1 BOTTOM RIGHT AS SEEN FROM FRONT-PANEL
FRONT-PANEL CONNECTOR
"WRITE" LED
"READ" LED
"POWER OK" LED
VN2222L
1N4148
LEDRD
LEDWR
POWEROK
FRONT-PANEL DISPLAY
SUBREFLECTOR CONTROL VME BOARD
Title
FRONT - PANEL : CONNECTOR AND DISPLAY
Size Document Number
B F. MOREL
REV
Date: August 8, 1995 Sheet 6 of 6

1.12 Submot Board layout:



1.13 Submot Board schematics:




SUBREFLECTOR CONTROL VME BOARD
Title
PIGGY BACK MOTOR BORDS : CONNECTORS
Size Document Number
A
F. MOREL
REV
Date: August 9, 1995 Sheet 2 of 2
DISPLAY
VCC
R1 470
R2 470
R3 470
R4 470
LED1 IDONE GREEN LED
LED2 SWI RED LED
LED3 ENA GREEN LED
LED4 RUN YELLOW LED
Q1 VN2222L
Q2 VN2222L
Q3 VN2222L
Q4 VN2222L
IDONE
SWI
ENA
RUN
/RESET
J1
3M 9120-4500JL
J2
3M 9134-4500JL
/RDAP
SIN
COS
SWI
ENA
PVR
NVR
WRTRP
IDONE
/MOVUP
/MOVDN
RUN
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13
ID14
ID15
CLKMOT
MALE CONNECTORS ON ETCH SIDE FIT FEMALE SOCKETS OF MOTHER BOARD