An Architecture for Integrating VLBI Digital Processing into the Next Generation IRAM PdBI Correlator

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Abstract

The next generation digital backend for the Plateau de Bure interferometer will be designed to provide phased-array data for millimeter VLBI observations. This report describes tied-array operation and the digital filtering scheme which generates baseband signals ready to be recorded in standard VLBI systems. An efficient polyphase implementation is proposed for that filtering module.

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1. Introduction

The next generation digital backend for the Plateau de Bure interferometer (PdBI) will include, apart from the local correlator engine, a specific digital system to perform global millimeter VLBI observations in a phased-array operation mode.

The idea is to generate VLBI-compatible data by processing the coherent addition of signals coming from each antenna digital frontend (also known as digital receiver).

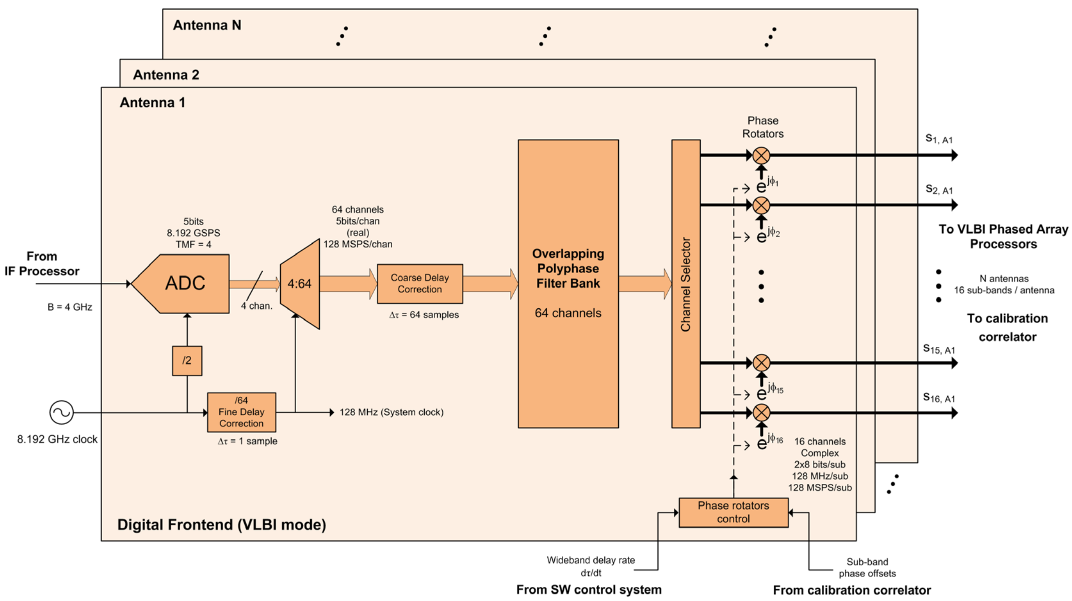

Figure 1: Digital Frontend (or Digital Receiver) for VLBI operation mode.

Figure 1 shows the proposed architecture for the digital frontend. Its preliminary specifications are the following:

- Sampling at 8.192 GSPS with 5 bits.
- Frequency demultiplexing scheme based on a 64-channel overlapping polyphase filter bank [1]. There is a frequency overlapping of 50 % to avoid spectral holes (see Figure 2). Output channels are complex-valued, requantized to 16 bits and the output rate is 128 MSPS (64 MHz of effective bandwidth, due to overlap).
- Frequency slice selector over the full 4GHz bandwidth. For VLBI full rate operation (4Gbps), 16 frequency windows must be processed in parallel.
- The FFT processors used in local FX-correlation mode are replaced by phase shifters in VLBI mode. These phase rotators allow the subsequent coherent addition of signals coming from the *N* antenna digital frontends at the same frequency slice (see Figures 1 and 3).

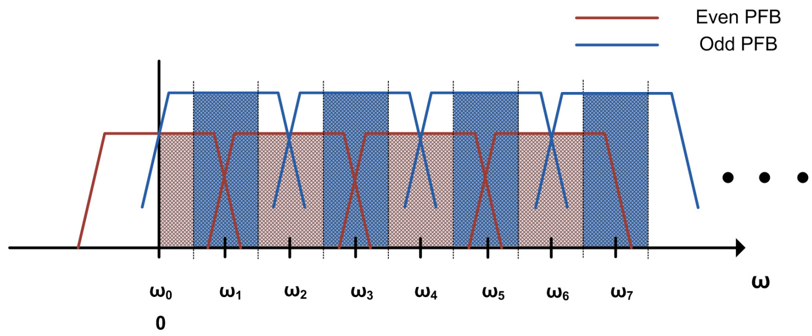

Figure 2: Overlapping polyphase filter bank frequency response. It is a combination of two conventional polyphase filter banks shifted by half a frequency channel.

2. Phased array operation

To perform VLBI-observations together with other telescopes around the world, the PdB interferometer must work like a single-element telescope in a phased-array operation. This means, the signals from the *N* antennas of the array must be coherently added to obtain a jointly response (improving the S/N ratio in a theoretical factor of *N*). Our system performs this summation for each selected sub-band, as it is shown in figure 3.

For a proper coherent addition, the relative phase between the antenna signals must be zero (within a tolerable error over the frequency range). This required phase correction is done by digital hardware and is usually known as digital beamforming. In our system, an improved time-domain beamformer is chosen. This beamformer contains, apart from the classical digital delay lines, a digital offset correction, which is carried out by phase rotators in an natural way due to the complex format at the output of the overlapping polyphase channelizer. Note that a frequency-domain beamformer is computationally more expensive since a FFT is needed for each antenna and an inverse FFT must be performed after the summation of the phased-corrected signals.

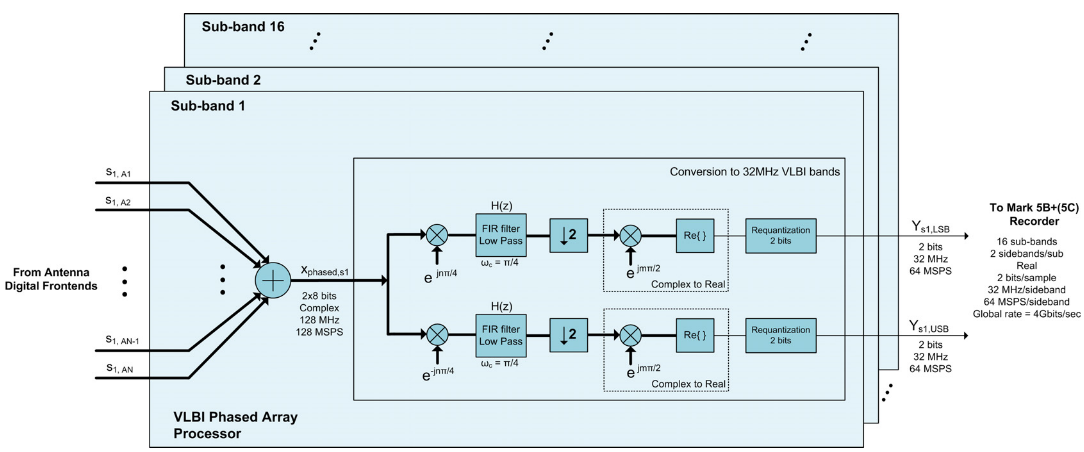

Figure 3: Phased array processors (adder and filtering module for 32MHz VLBI bands).

2.1. Delay and phase offset corrections

2.1.1. Delay correction

A digital delay of D samples ($D \cdot Ts$ seconds) between two antennas is equivalent to a slope of $-2\pi D/f_S$ [radians/Hz] in the phase curve versus the analog input frequency. For a correct local interferometer operation of the telescope, geometrical, instrumental and atmospherical relative delays between every pair of antennas must be calibrated. In a phased-array mode, for a proper coherent addition of the signals received at the antennas, apart from the delay compensation, it is necessary to maintain the phase offsets between the signals equal to zero. This offset correction is explained in the next section.

The delay compensation is proposed to be carried out by the digital receiver before the filter bank channelizer. That means, the delay is corrected over the entire 4GHz band. To get a proper accuracy, one module will do the fine delay correction and another one will be used for the coarse one (see figure 1).

For fine delay correction, a simple mechanism will be used to get delay steps of 1 sample (0.122 ns). It will be implemented by the low-frequency clock generation system (one for each digital frontend), which divides the sampling frequency by a factor of 64 to generate the 128 MHz clock signal (system-clock). The delay is performed by changing the relative phase between the input (8.192 GHz) and the output low-frequency clock. 64 different phase values around the output clock period are available. As the high frequency clock is common for all the antenna digital receivers, this phase values correspond to relative delays between antenna signals from 0 to 7.8125 ns (output clock period), in steps of 0.122 ns.

Coarse delay correction is performed just after the time demultiplexer (to 64 lines) and before the overlapping polyphase filters. It will be implemented using RAM memory resources of the digital frontend FPGA. Input data, organized in words of 64 samples, will be stored in memory at 128 MHz clock frequency. Changing the output memory address, delay steps of 64 samples or 7.8125 ns are obtained. The memory size will be selected taking into account the geometry of the interferometer.

2.1.2. Phase offset correction

A digital phase rotator compensates phase errors within each selected sub-band coming from the overlapping channelizer (see figure 1). This phase offset can be divided into a component proportional to the delay error (subsampling delay) and another residual component related to the phase frequency response of the receiver chain (group delay instrumental imperfections):

$$\tau_k(t) = \phi_k(\tau_{error}) + \phi_{k,residuel} \qquad k = 0, 1, \ldots, 63\,; \tag{1}$$

where k is the channel index. It is assumed that the group delay is constant over the sub-band frequency range.

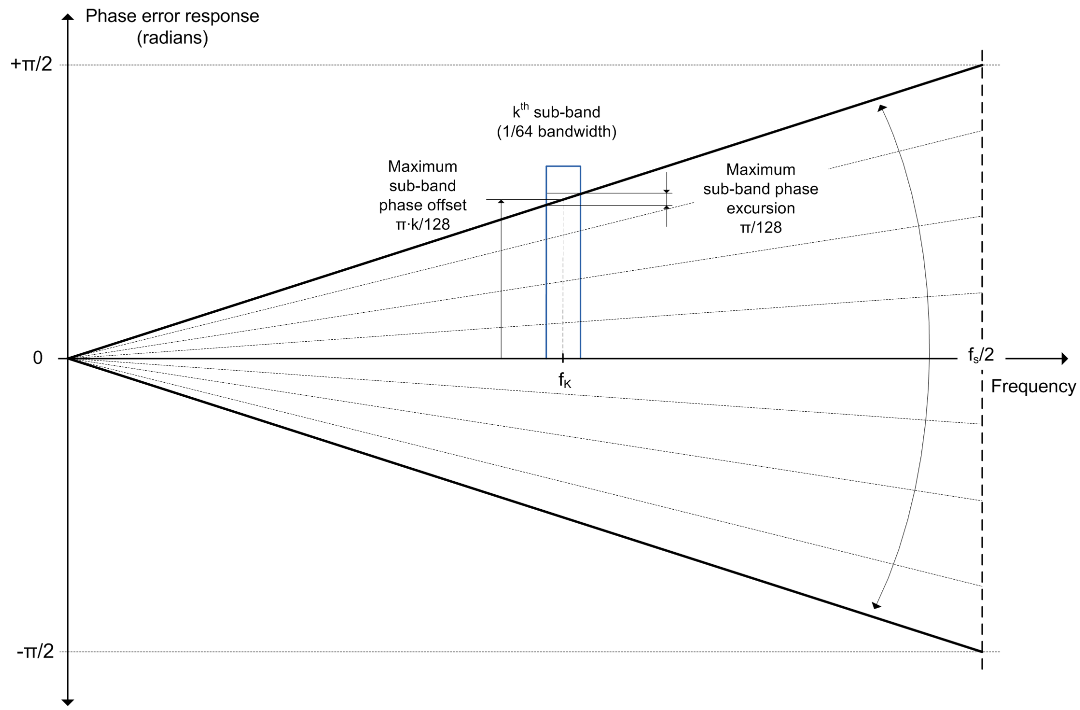

Figure 4: Phase error response of a wideband antenna signal.

Figure 4 shows the phase response for one antenna signal, after the integer delay and its residual phase component are corrected. As the delay resolution is 1 sample, the phase error curve is a line with a slope value between $+\pi/fs$ and $-\pi/fs$ (delay error of -0.5 and +0.5 samples, respectively).

As the astronomical source moves across the sky due to earth rotation, the phase error slope swings continuously between both limit slopes. Maximum phase excursion for the whole wideband signal is +/- $\pi/2$ radians. However, as the subsequent processing is done at sub-band level (64 channels in our case), the phase excursion is reduced to a range +/- $\pi/256$ radians around the phase offset at the channel center frequency (denoted as $\phi_k(\tau_{\text{error}})$ in equation 1). This phase offset is proportional to the channel index and to the delay error:

$$\phi_e^k(t) = -\frac{\pi}{N_C} \cdot D_e(t) \cdot k, \qquad k = 0, 1, ..., N_C\text{-}1; \tag{2}$$

The number of overlapping channels N_C is 64 in our case; and D_e denotes the delay error normalized to the sampling period ($-1<D_e<1$). Therefore, D_e represents the subsampling delay that is not corrected but must be tracked in order to compensate the sub-band phase offset.

Maximum phase offset is +/- $\pi \cdot k/128$ for the k-th sub-band. To allow precise offset correction, the phase rotators will take discrete values multiple of $\pi/128$ using 16 bits to quantize the complex exponential value (8 bit for real and imaginary components).

For the PdB interferometer, a maximum delay rate of approximately +/-0.5 ns/s is foreseen; corresponding to an east-west antenna spacing of 2 km. It is equivalent to a normalized delay rate ($\Delta D_e/\Delta t$) of approximately 4 units per second (or 4 Hz). The sub-band phase rate is also proportional to the channel index, and is computed as:

$$\frac{\Delta\phi_e^k}{\Delta t} = -\frac{\pi}{N_C} \cdot \frac{\Delta D_e}{\Delta t} \cdot k, \qquad k = 0, 1, ..., N_C\text{-}1; \tag{3}$$

Using practical values for our system, the maximum sub-band phase rate is:

$$\left.\frac{\Delta\phi_e^k}{\Delta t}\right|_{\max} \approx -\frac{\pi}{16} \cdot k, \qquad k = 0, 1, ..., 63; \tag{4}$$

As the phase (delay) rate depends on antenna and astronomical source positions, a system called phase rotators control (see figure 1) must select for each sub-band the proper phase value at a rate estimated by software (maximum rate of aprox. 4 Hz for the last channel). This control module will be implemented using numeric controlled oscillators (NCO) to generate different rates for each sub-band and look up tables where the complex exponential values for each phase will be stored.

Concerning the summation efficiency, the maximum phase excursion due to delay error and the maximum phase offset compensation error are both +/- $\pi/256$ radians. Therefore, the maximum phase error between two signals before the addition is +/- $\pi/128$ radians, which is equivalent to a coherence factor of approximately 99.97%.

3. Conversion to VLBI baseband channels

3.1. Architecture description

Once the phased-array summation is done, each resulting phased sub-band must be processed to satisfy standard VLBI recording specifications. The Mark 5C disk-based VLBI data recorder will increase the recording rate capability to 4096 Mbps [2]. It will accept VDIF[1] formatted [3] data from a standard 10 Gigabit Ethernet connection.

Typically, recorded data will be split into 32 non-overlapped real-valued sub-bands of 32-MHz each and requantized to 2 bits/sample, achieving a maximum rate of 4Gbps. VDIF standard considers other combinations of channel resolution and number of bits per sample.

Figure 5 illustrates the conversion process for a generic number of output VLBI baseband signals. The idea is to divide the useful frequency range of a 128-MHz phased overlapping sub-band into *M* contiguous *non-overlapping* channels. *M* is assumed to be a power-of-two number.

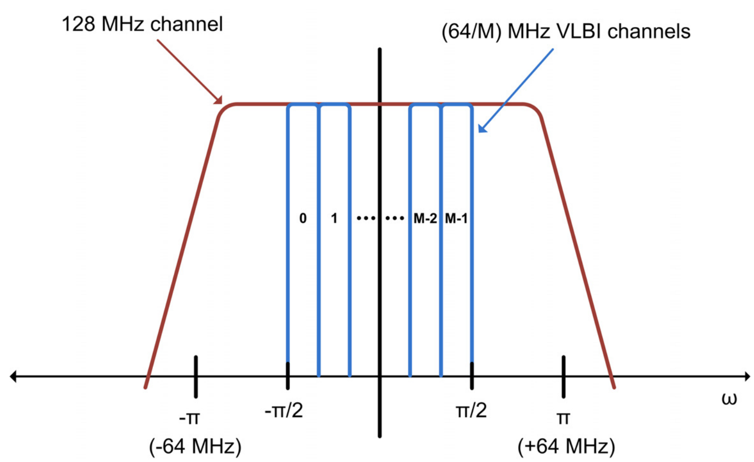

Figure 5: Illustration of the conversion from a phased overlapping sub-band to *M* VLBI baseband signals.

3.1.1. Case of 32 MHz bands

For the typical case of 32-MHz bands, two output baseband signals must be obtained for each phased overlapping sub-band (see figure 3). These two output bands are known as lower and upper sidebands (LSB and USB). Therefore, 16 overlapping channels must be processed to reach the full-capability recording of 4Gbps.

Figure 6 shows the signal processing architecture, proposed to generate two 32-MHz VLBI channels from one 128-MHz complex-valued overlapping channel coming from

[1] VDIF: VLBI Data Interchange Format

the phased-array adder. Each branch consists on a digital base band converter (DBBC), followed by a complex-to-real converter and a requantization block.

Actually, the input complex signal is frequency-translated in order to place the center frequency of each sideband to DC. Next, a low-pass FIR filter selects the desired frequency band and a decimator-by-two block expands the spectra leaving free half of the frequency range for the following complex to real conversion. Finally a requantization to 2 bits per sample is done.

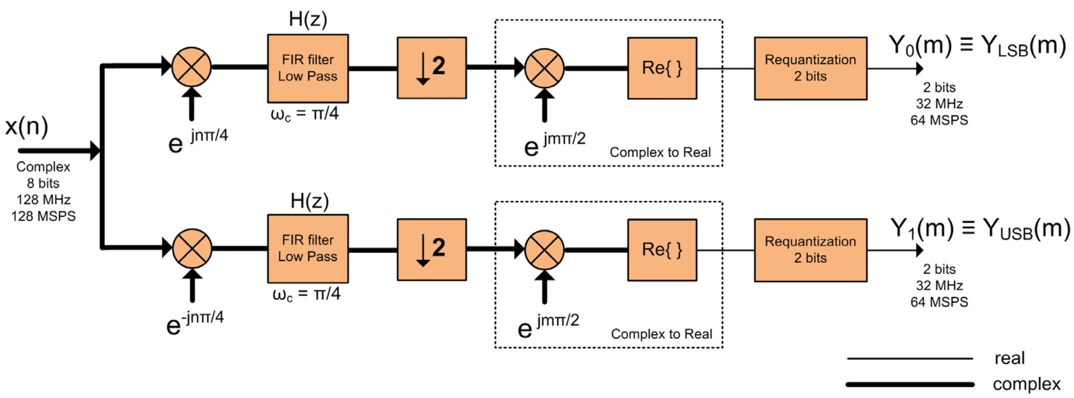

Figure 6: Signal Processing architecture to generate 32MHz VLBI baseband signals from a single phased overlapping sub-band.

3.1.2. Generic case (M output channels)

Figure 7 shows the generic DSP architecture to generate M (power-of-two number) output channels. The central angular frequencies (in radians/sample) for the VLBI output channels are:

$$\omega_k = \frac{\pi}{2M}(2k - M + 1); \qquad k = 0, 1, \ldots, M-1; \tag{5}$$

where a frequency-increasing scheme for channel labeling is used (as is represented in Figure 5).

Modules with M = 4, 8, 16 and 32 channels must be used to achieve VLBI channel bandwidths of 16, 8, 4 and 2 MHz, respectively. In practice, a different programming core will be loaded to the FPGAs for each VLBI recording mode.

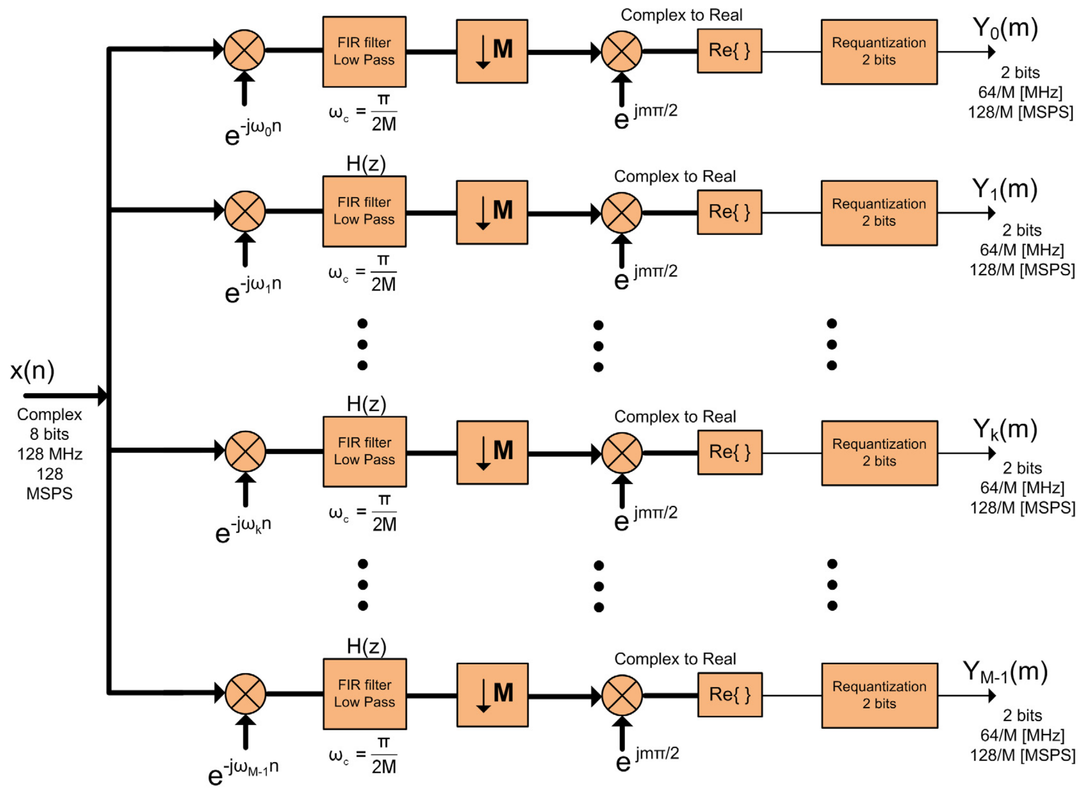

Figure 7: Signal Processing architecture to generate *M* VLBI baseband signals from a single phased overlapping sub-band.

3.2. Polyphase implementation

This VLBI conversion module has characteristics like uniform-placed channel central frequencies, low pass FIR filters and multirate conversion, which suggest using a polyphase-type implementation. Polyphase systems are high-efficient structures in terms of saving logic-elements and power consumption [4].

Our particular polyphase architecture will integrate both the DBBCs and the complex-to-real converters. Requantization blocks will be connected to the outputs of this module in order to generate a signal stream ready to be formatted and transmitted to the Mark-5C VLBI recording system.

Figure 8 shows the block diagram for the polyphase implementation. It consists of a polyphase filtering stage followed by a Fourier transform module and a complex to real conversion block. Unlike the classical polyphase uniform filter bank, this implementation processes only the central (useful) range of the input frequency spectra in order to generate *M* equal-spaced non-overlapping output channels (real-valued for this particular case). As a result, the expressions to describe the system will be more complex than the classical ones.

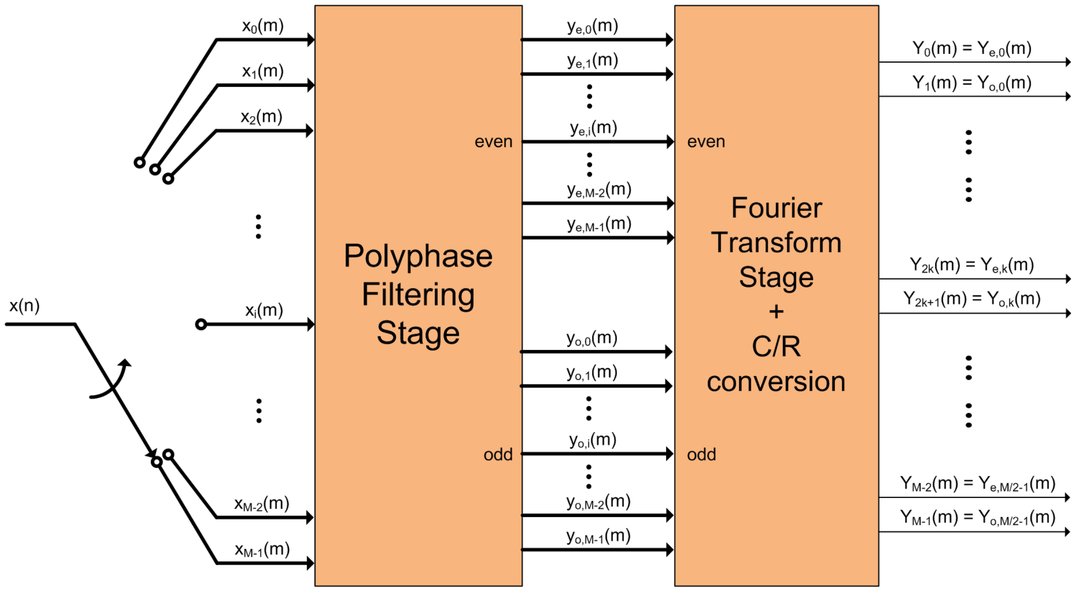

Figure 8: Polyphase implementation for the conversion to VLBI signals (*M* channels).

3.2.1. Polyphase filtering stage

Filtering stage is divided into *M* polyphase filtering blocks. Each filtering block is a combination of two FIR polyphase filters. They are known as even and odd polyphase filters since first one only contributes to global even output channels and the other one only to odd ones. Output complex signals for the filtering stage are computed as:

$$\begin{aligned} y_{e,i}(m) &= \sum_{r=0}^{L-1} h_i^e(r)\cdot x_i(m-r); \qquad i=0,1,\dots,M-1 \\ y_{o,i}(m) &= \sum_{r=0}^{L-1} h_i^o(r)\cdot x_i(m-r); \qquad i=0,1,\dots,M-1 \end{aligned} \tag{6}$$

where m is the time index, $L\,(=N/M)$ is the number of coefficients for each polyphase filter; $h_i^e(r)$ and $h_i^o(r)$ are the impulse response for the *i*-th even and the *i*-th odd polyphase filter, respectively. A counterclockwise commutator model (see figure 8) is used: $x_i(m)=x([M-1-i]\cdot m)$.

As for the classical uniform filter bank, the impulse responses of the polyphase filters are decimated (by a factor *M*) versions of the impulse response of the low-pass prototype filter '*g*(*n*)' (*N* coefficients). However, for this particular case, the decimated versions are modulated by complex signal and are phase shifted (by a constant value). That implies that filter coefficients are complex-valued. The impulse responses for the even and odd polyphase filters are:

$$h_i^e(r) = e^{-j\frac{\pi}{2M}(M-1)i} \cdot \{g(M \cdot r + i) \cdot e^{-j\frac{\pi}{2}(M-1)r}\};$$
$$h_i^o(r) = e^{-j\frac{\pi}{2M}(M-1)i} \cdot \{g(M \cdot r + i) \cdot e^{-j\frac{\pi}{2}(M-1)r}(-1)^r\} \quad (7)$$

where $r = 0, 1, ..., N/M - 1$ and $i = 0, 1, ..., M - 1$.

According to the previous equation, for the same branch (i index), filter coefficients of the even and odd filters are equal in absolute value. Actually, even-indexed coefficients are equal and odd-indexed coefficients have opposite values:

$$h_i^e(2p) = h_i^o(2p); \qquad p = 0, 1, 2, ..., \frac{N}{2M} - 1$$
$$h_i^e(2p+1) = -h_i^o(2p+1); \qquad p = 0, 1, 2, ..., \frac{N}{2M} - 1 \quad (8)$$

Thus, combining equations 6 and 8:

$$y_{e,i}(m) = \sum_{p=0}^{L/2-1} h_i^e(2p) \cdot x_i(m-2p) + \sum_{p=0}^{L/2-1} h_i^e(2p+1) \cdot x_i(m-2p-1)$$
$$y_{o,i}(m) = \sum_{p=0}^{L/2-1} h_i^e(2p) \cdot x_i(m-2p) - \sum_{p=0}^{L/2-1} h_i^e(2p+1) \cdot x_i(m-2p-1) \quad (9)$$

where $p = 0, 1, 2, ..., \frac{N}{2M} - 1$ and $i = 0, 1, ..., M - 1$.

Therefore, the filter multipliers are shared between even and odd filters for each branch or filtering block. Figure 9 shows the diagram for one branch. Note that both register and arithmetic modules work in complex-arithmetic.

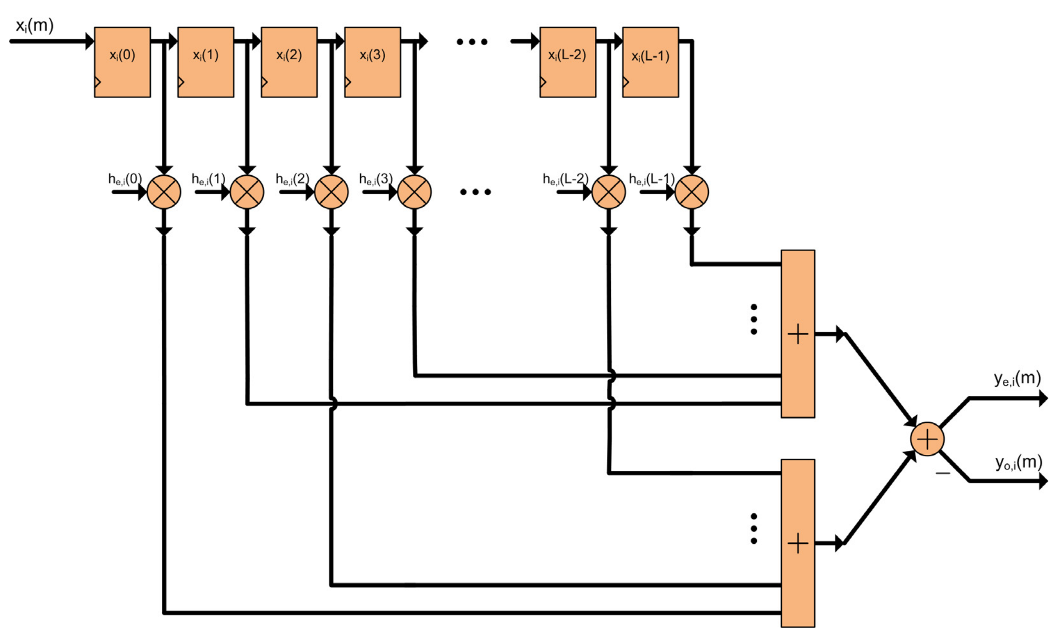

Figure 9: Polyphase filtering module ($L=N/M$).

3.2.2. Fourier transform stage and complex-to-real conversion

Following the polyphase filters, signals are processed by a module that is based on Fourier transform blocks. In addition, this module integrates the complex-to-real conversion which is needed to fulfill VLBI format specifications. Figure 10 shows the block diagram for this last stage of the polyphase implementation.

At first, we have two inverse M-point Fast Fourier Transform (IFFT) engines, one for each group of M channels (even and odd) coming from the polyphase filtering stage. Each odd input is phase shifted by a complex exponential signal. Only half-output channels are used from each IFFT block. Thus, output signals for the IFFT engines are:

$$\begin{aligned} \hat{Y}_{e,k}(m) &= \hat{Y}_{2k}(m) = \sum_{i=0}^{M-1} y_{e,i}(m)\cdot e^{+j\frac{2\pi}{M}k\cdot i}; \qquad k = 0,1,2,\ldots,M/2-1 \\ \hat{Y}_{o,k}(m) &= \hat{Y}_{2k+1}(m) = \sum_{i=0}^{M-1} y_{o,i}(m)\cdot e^{+j\frac{\pi}{M}i}\cdot e^{+j\frac{2\pi}{M}k\cdot i}; \qquad k = 0,1,2,\ldots,M/2-1 \end{aligned} \tag{10}$$

Later, a modulation and a real part operator are applied to IFFT outputs in order to generate the global output channels of the conversion system:

$$\begin{aligned} Y_{2k}(m) &= Y_{e,k}(m) = \mathrm{Re}\left\{\hat{Y}_{2k}(m)\cdot e^{-j\cdot\pi\cdot 2k\cdot m}\cdot e^{+j\frac{\pi}{2}M\cdot m}\right\}; \qquad k = 0,1,2,\ldots,\ M/2-1 \\ Y_{2k+1}(m) &= Y_{o,k}(m) = \mathrm{Re}\left\{\hat{Y}_{2k+1}(m)\cdot e^{-j\cdot\pi\cdot(2k+1)\cdot m}\cdot e^{+j\frac{\pi}{2}M\cdot m}\right\}; \qquad k = 0,1,2,\ldots,M/2-1 \end{aligned} \tag{11}$$

Without loss of generality, M is assumed to be a power-of-two number (as it is always for our backend). Then, two cases must be mentioned:

- M = 2 (32-MHz case). Eq. 11 is simplified as:

$$\begin{aligned} Y_{2k}(m) &= \mathrm{Re}\left\{\hat{Y}_{2k}(m)\right\}\cdot(-1)^m; \qquad k = 0,1,2,\ldots,M/2-1 \\ Y_{2k+1}(m) &= \mathrm{Re}\left\{\hat{Y}_{2k+1}(m)\right\}; \qquad k = 0,1,2,\ldots,M/2-1 \end{aligned} \tag{12}$$

- M > 2 ($M = 2^x$), that is represented in figure 10. Output signals are computed as:

$$\begin{aligned} Y_{2k}(m) &= \mathrm{Re}\left\{\hat{Y}_{2k}(m)\right\}; \qquad k = 0,1,2,\ldots,M/2-1 \\ Y_{2k+1}(m) &= \mathrm{Re}\left\{\hat{Y}_{2k+1}(m)\right\}\cdot(-1)^m; \qquad k = 0,1,2,\ldots,M/2-1 \end{aligned} \tag{13}$$

These output baseband signals must be requantized to 2 bits, in order to have compatible channels ready to be transmitted to the Mark-5C VLBI recorder.

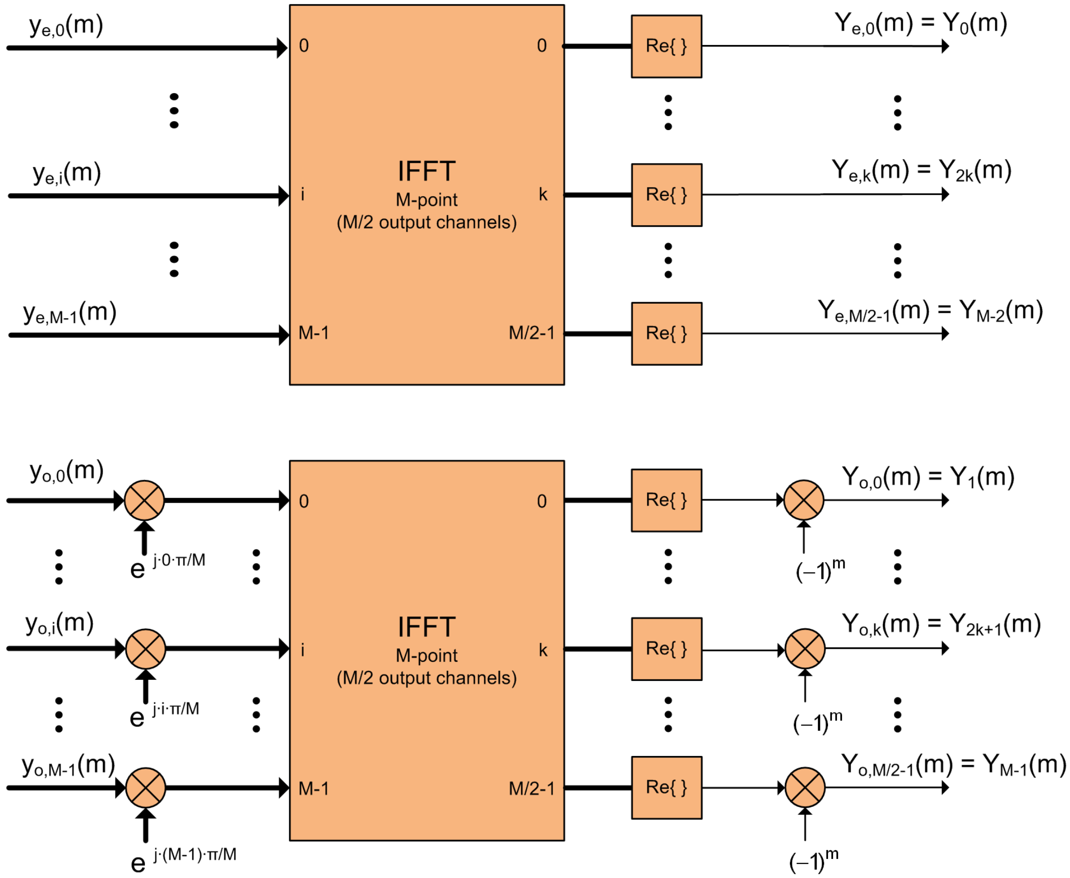

Figure 10: Fourier transform stage and Complex to Real conversion for $M > 2$ ($M = 2^x$)

3.3. Simulations

Polyphase VLBI conversion structures, for different number of channels, were validated using Matlab numerical computing package. Figure 11 shows simulation results for the 32-MHz case (2 output subbands). 256 coefficients, quantized to 10 bits, are used for the prototype FIR filter.

The frequency response for 8-MHz output bands (M=8) is shown in figure 12. For this case, 512 coefficients are used for the low-pass filter to achieve an out-band rejection of approximately -60 dB.

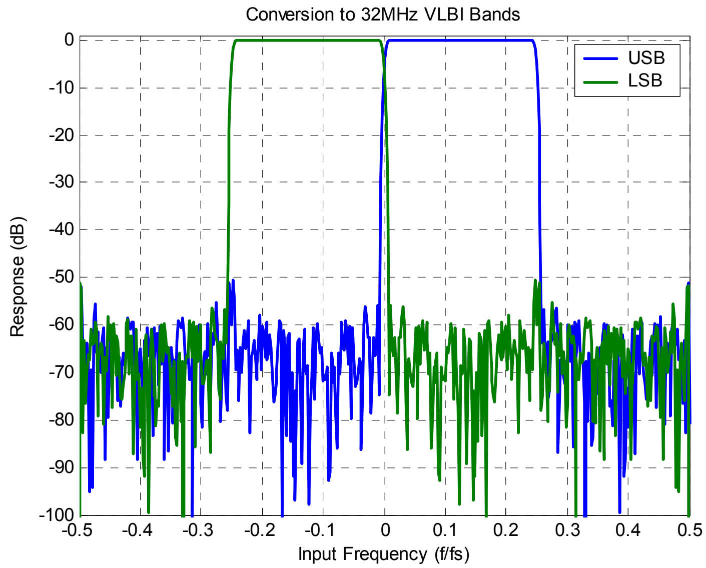

Figure 11: Simulation results for 32-MHz VLBI basebands.

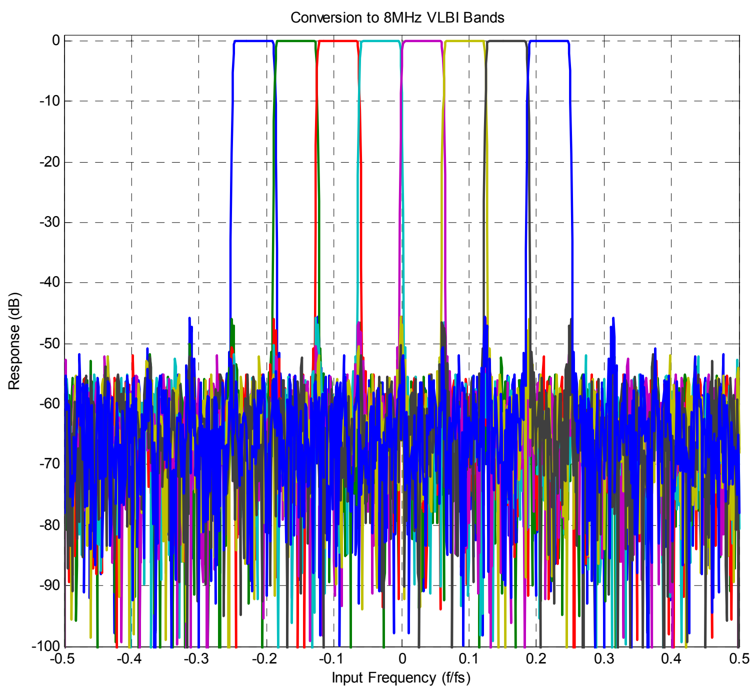

Figure 12: Simulation results for 8-MHz VLBI basebands.

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