



IRAM-COMP-023

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VME board SYNC

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REVISION	DATE	AUTHOR	SECTION/PAGE AFFECTED	REMARKS

Content

1	VME board “SYNC”	3
1.1	Description:.....	3
1.2	Functionalities:.....	3
1.3	Accessing the board:.....	3
1.4	Interrupts:.....	3
1.5	Switches:	4
1.6	Front-panel:	5
1.7	Schematics:	6

1 VME board "SYNC"

1.1 Description:

This module allows synchronization of all the antennas of the interferometer, using the "1 SEC" pulse of the "TIME" Bus on the Plateau de Bure.

The "1 SEC" pulse (40 usec *measured* duration) leading edge is synchronous with each "SECOND" change of the Observatory Clock, supplied by a GPS receiver.

The board is configurable with switches, as described in section 1.5, and visible on sheets 3 and 4 of the schematic drawings.

1.2 Functionalities:

This board detects the "1 SEC" Pulse supplied by the "TIME" Bus and generates an interrupt (IT "SLO") each time it receives this pulse.

If the "1 SEC" pulse is missing OR late OR early (tolerance: +/- 8 msec), OR if there are extra pulses, the board generates another interrupt (IT "ERR").

Using an internal crystal oscillator, it interpolates between "1 SEC" pulses, generating a selectable frequency (32, 64, 128, 256 Hz) resynchronized on each "1 SEC" pulse.

It generates a 3rd interrupt (IT "FAST") on each leading edge of this internal frequency.

It also counts this frequency, allowing the user to read the time elapsed between two "1 SEC" pulses, with a resolution = (1 second / N), N being the selected frequency.

1.3 Accessing the board:

Only one 16-bit read-only register is accessible, at Board Base-Address.

This address is switch-selectable (see section "Switches" below). The 16-bit register only is readable in Short Mode (Address on 16 bits, Address Modifier = 29 or 2D).

It contains the time elapsed since the last "1 SEC" pulse.

Bit 15 ("ERR") is set if the board is not synchronized with the "1 Hz" pulse.

Readout format of the data depends on the selection made with switch RC1 ("Mode" switch).

-DATA FORMAT (unit is 1 second, default is RC1 =1):

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RC1=3	ERR	0	0	0	0	0	0	0	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256
RC1=2	ERR	0	0	0	0	0	0	0	1/2	1/4	1/8	1/16	1/32	1/64	1/128	
RC1=1	ERR	0	0	0	0	0	0	0	0	1/2	1/4	1/8	1/16	1/32	1/64	
RC1=0	ERR	0	0	0	0	0	0	0	0	0	1/2	1/4	1/8	1/16	1/32	

1.4 Interrupts:

This board generates 3 interrupts.

All of them use the same VME IRQ level (IRQ 4), but each interrupt uses its own unique vector.

IT "ERR" is generated if the "1 SEC" pulse is missing or out of time.

IT "SLO" is generated upon receipt of EACH "1 SEC" pulse.

IT "FAST" rate depends on the position of RC1:

RC1 = 3 => IT FAST = 256 Hz.

RC1 = 2 => IT FAST = 128 Hz.

RC1 = 1 => IT FAST = 64 Hz (DEFAULT).

RC1 = 0 => IT FAST = 32 Hz.

Their relative priority is following:

IT "ERR" has highest priority and sends vector (VBASE + 2).

IT "SLO" has mean priority and sends vector (VBASE + 1).

IT "FAST" has lowest priority and sends vector (VBASE + 0).

Vector Base (VBASE) is defined with switch RC2 (switch "VEC", value from 0x0 to 0xF):

RC2	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
VBASE	F0	E0	D0	C0	B0	A0	90	80	70	60	50	40	30	20	10	0

1.5 Switches:

RC1: (MODE) Data Format and Interrupt rate select (see above).

RC2: (VEC) Vector Base VBASE select (see above).

RC3: Board Base Address bits [11-8].

RC4: Board Base Address bits [15-12].

1.6 Front-panel:

From Top to Bottom:

Led “IT” (red) turns ON each time an interrupt is generated, and turns OFF when the interrupt is acknowledged.

Led “R/W” (yellow) flashes any time the board is accessed through the Bus.

Led “Synchro/Error” (red/green)

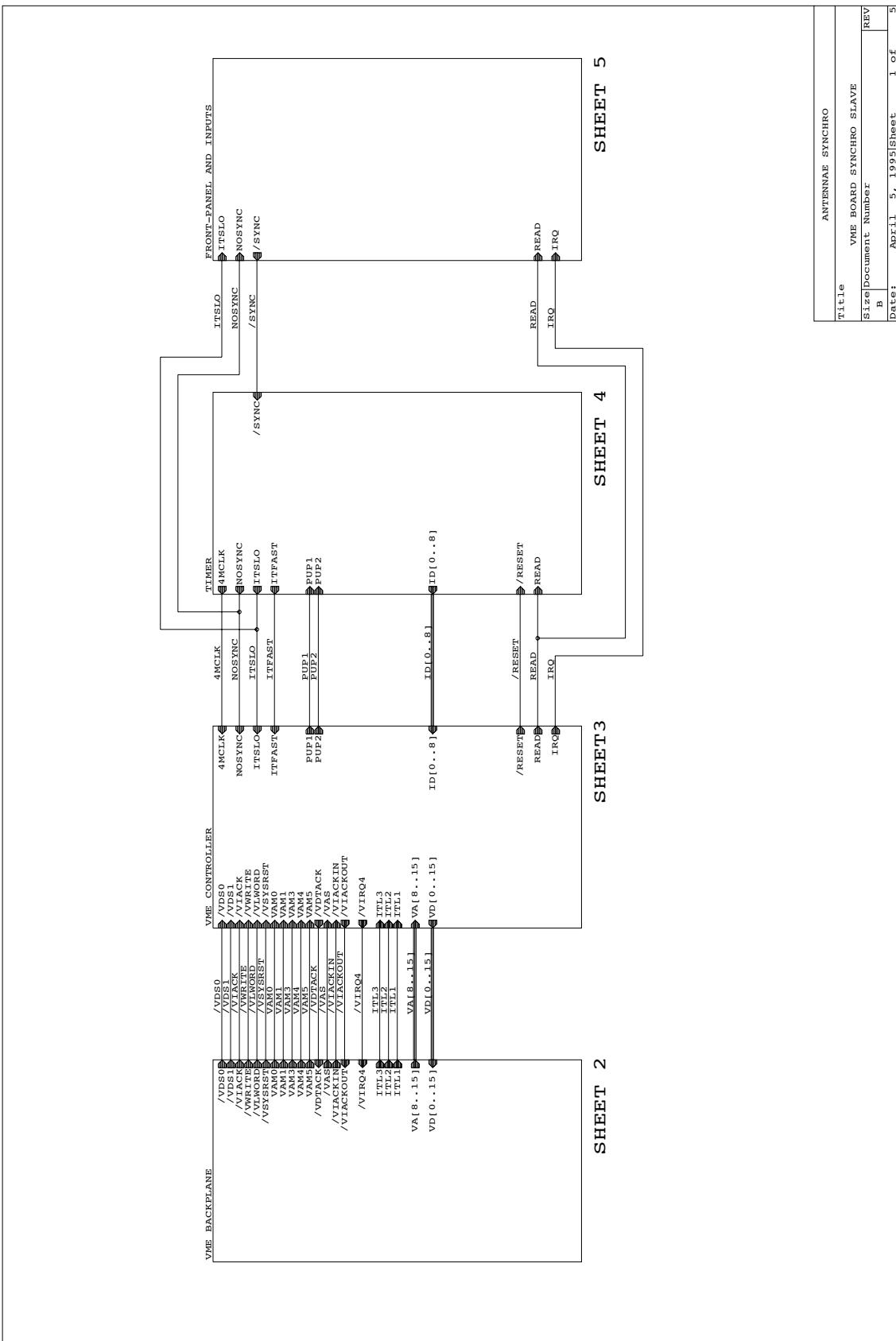
flashes green upon receipt of EACH "1 SEC" pulse .
turns ON red if the "1 SEC" pulse is missing or out of time,
and is reset by next "1 SEC" pulse , IF IN TIME.
Bit ERROR is set when LED SYNC/ERROR is red .

UNDER NORMAL CIRCUMSTANCES, NO RED LED SHOULD STAY ON.

CONNECTOR J1: Isolated BNC female connector.

Center pin: "1 SEC" PULSE +
Shield: "1 SEC" PULSE _ .

1.7 Schematics:



ANTENNAE SYNCHRO	
Title	VME BOARD SYNCHRO SLAVE
Size B	Document Number

Date:	April 5, 1995	Sheet	1 of 5
REV			

